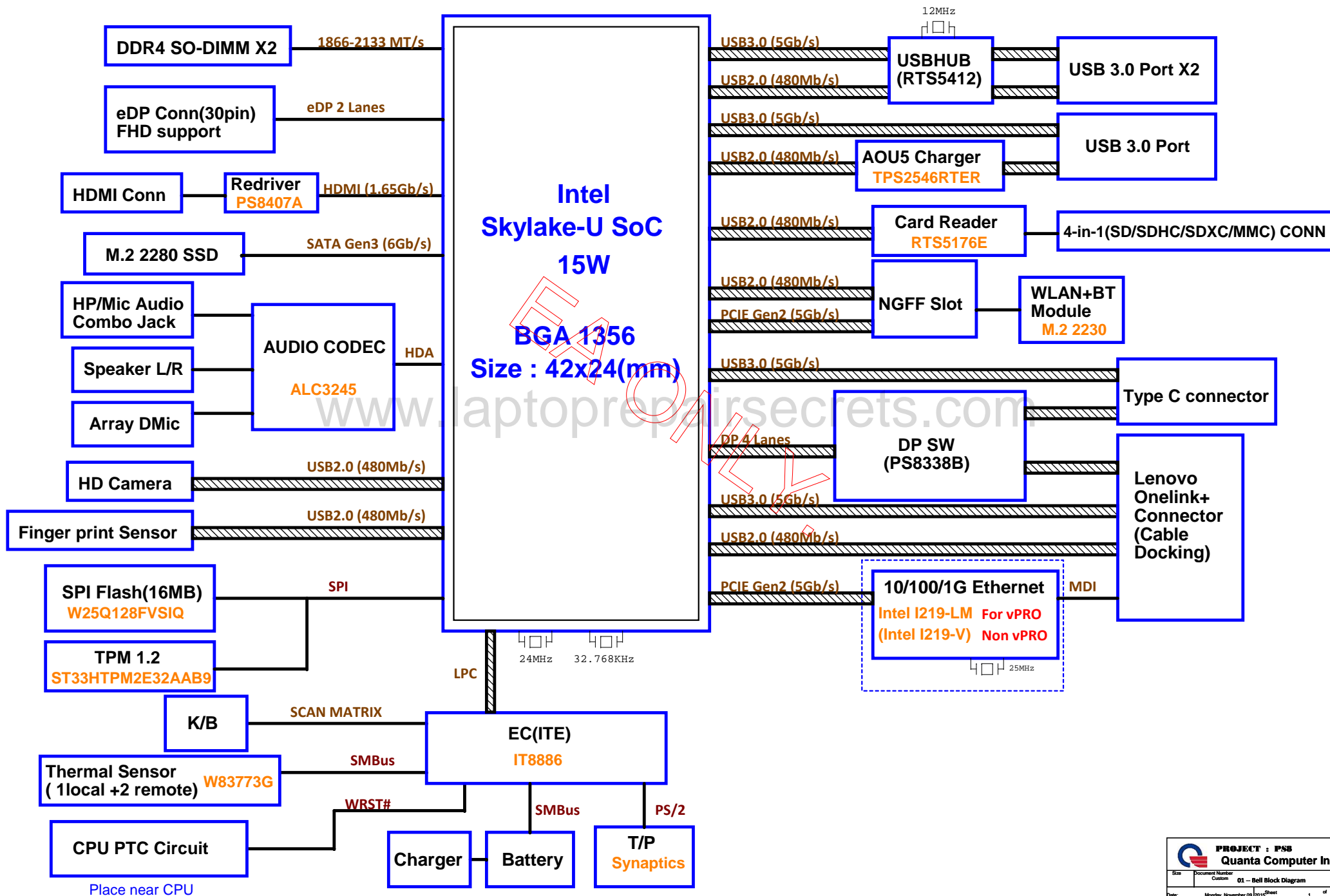


Intel Skylake-U Platform UMA Block Diagram (Windows)

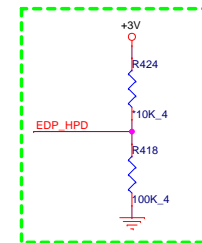
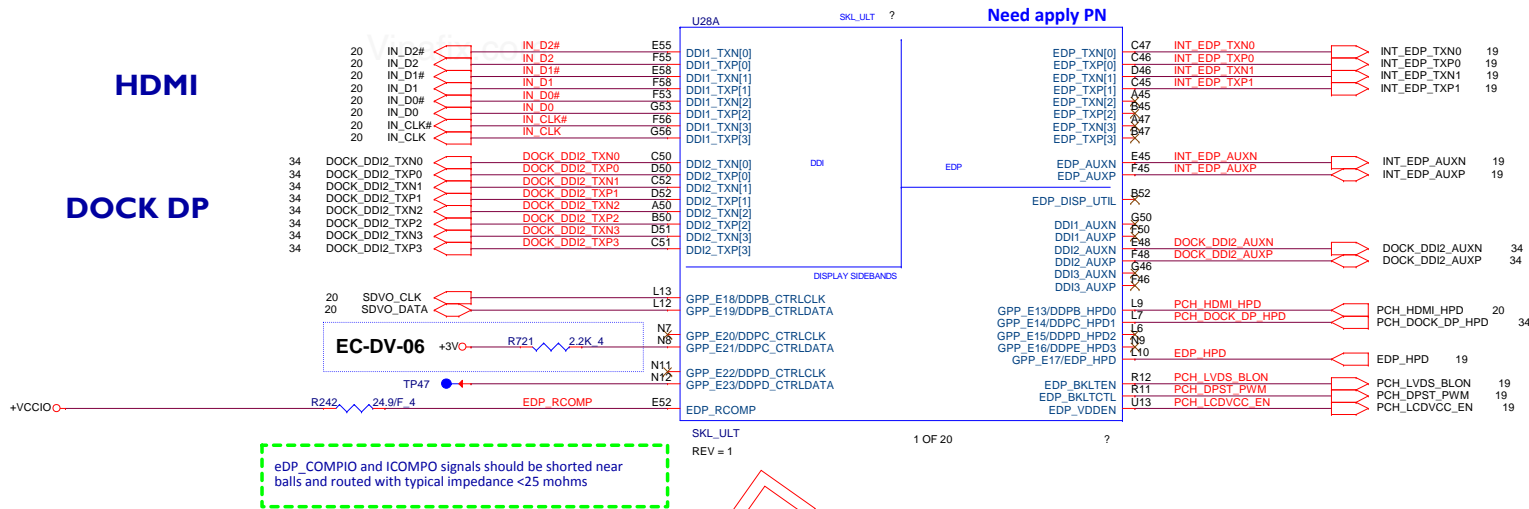


HDMI

DOCK DP

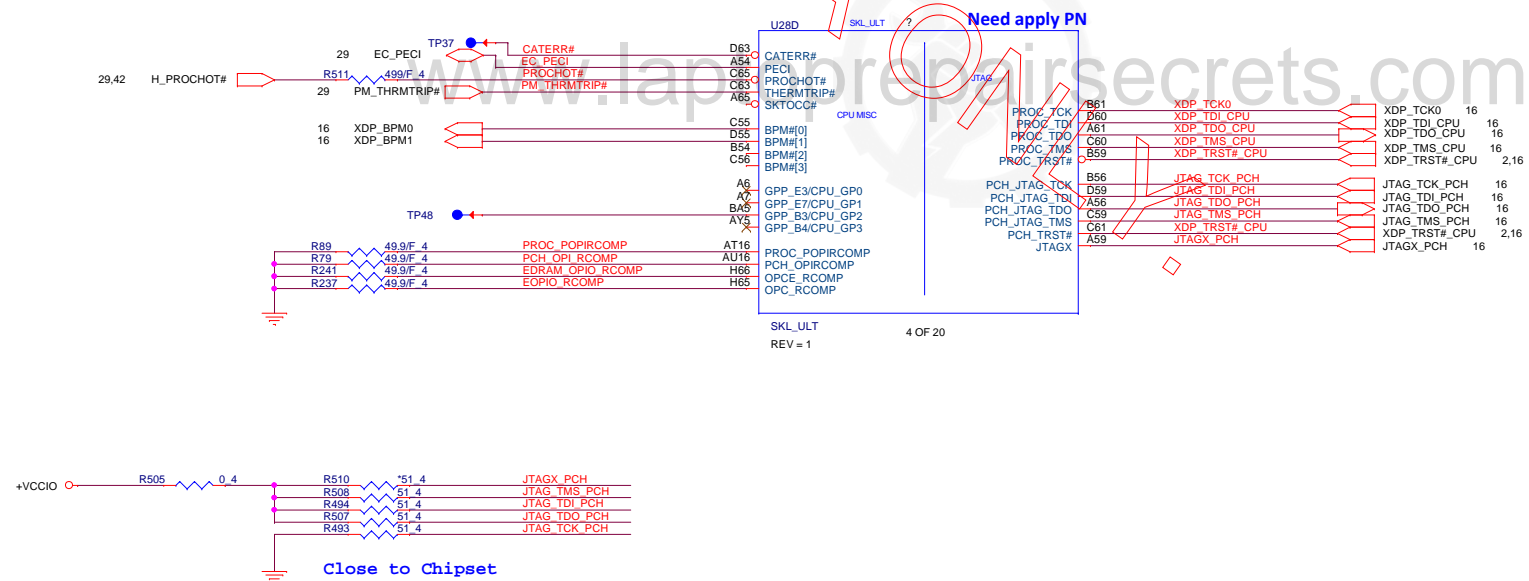
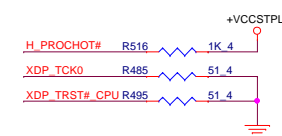
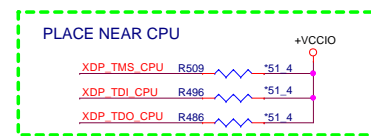
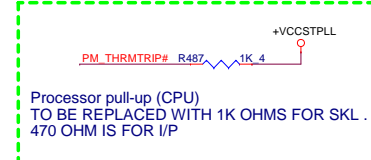
Need apply PN

Reserve EDP_HPD opposites circuit!



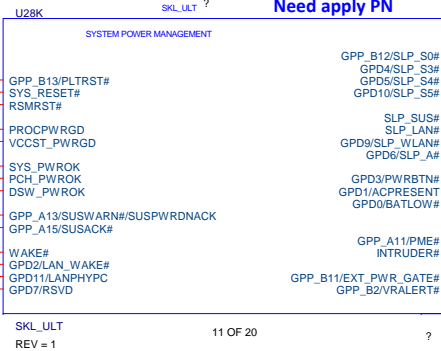
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Need apply PN

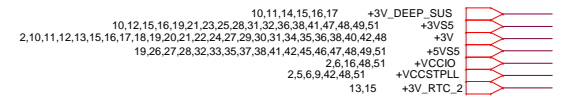
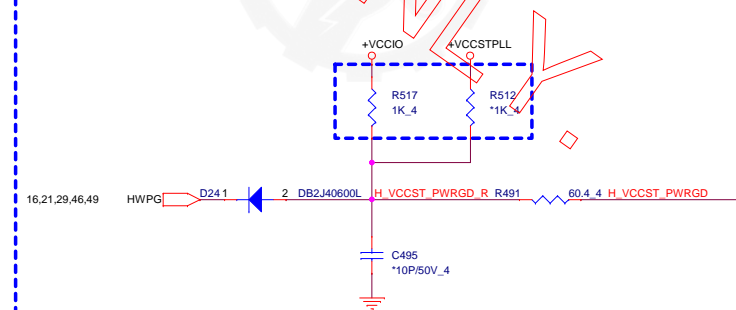


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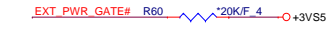
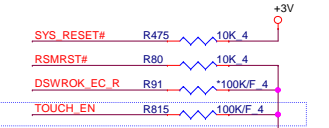
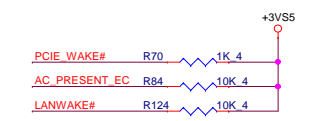
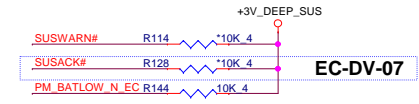
Need apply PN



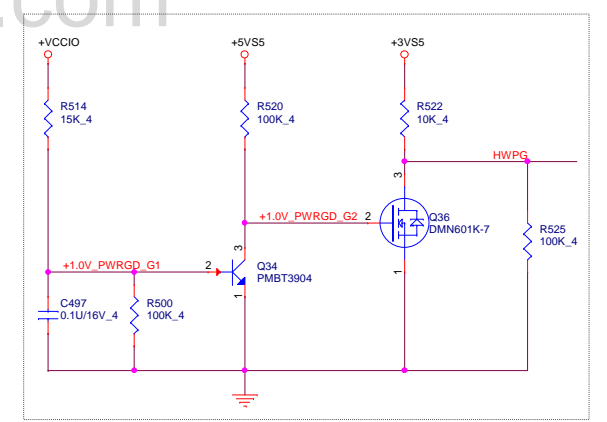
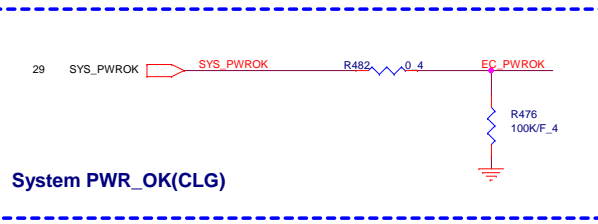
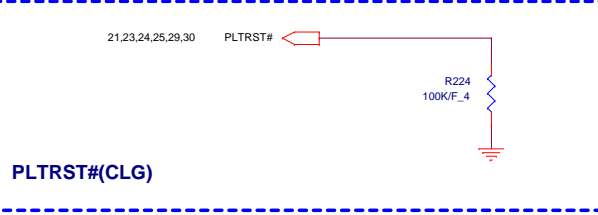
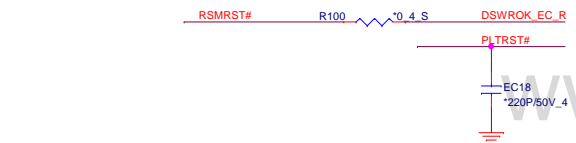
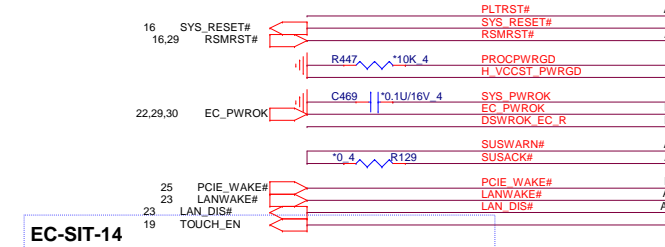
Close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"

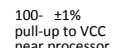


PCH Pull-high/low(CLG)




EC-SIT-14

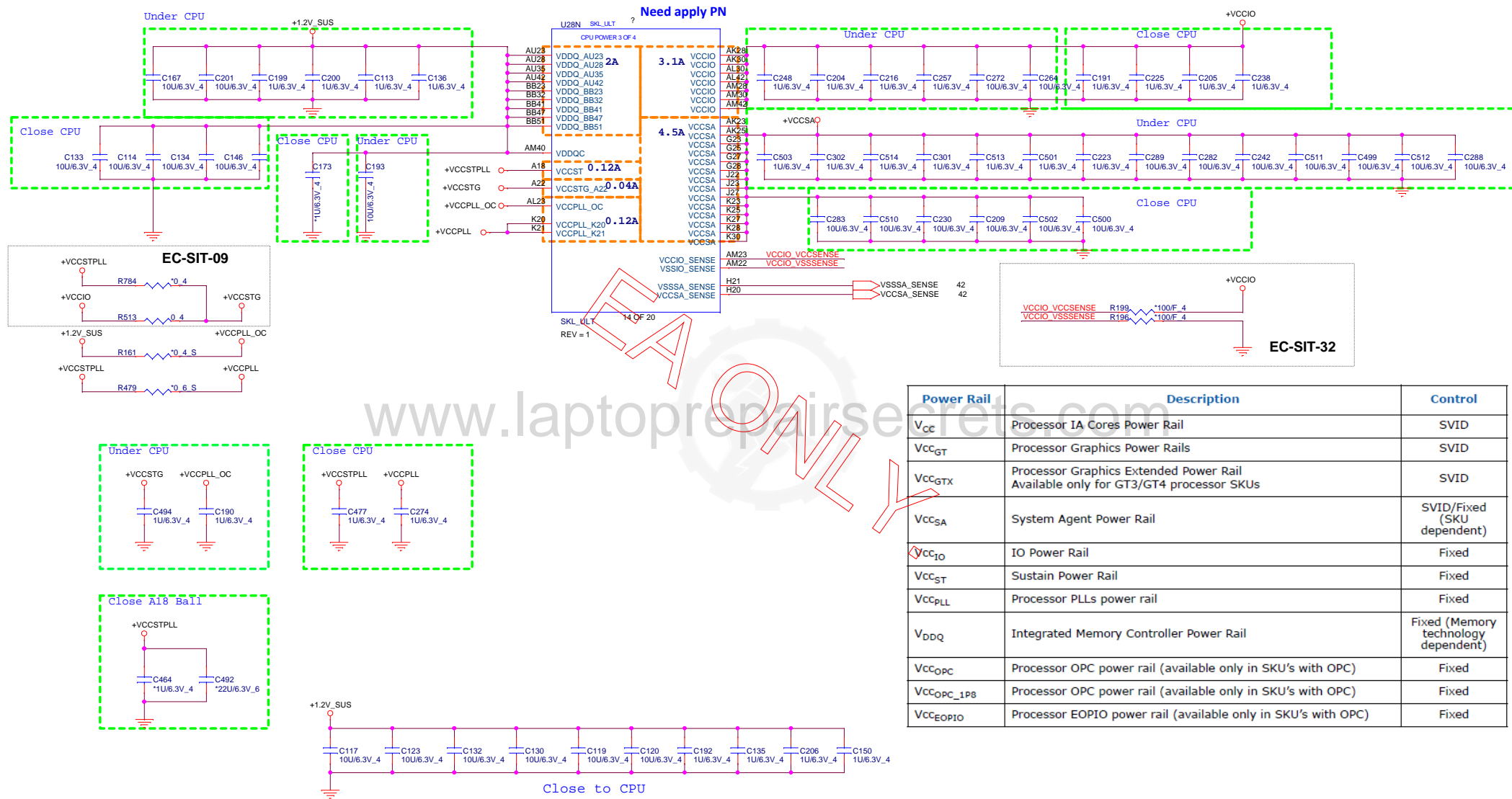




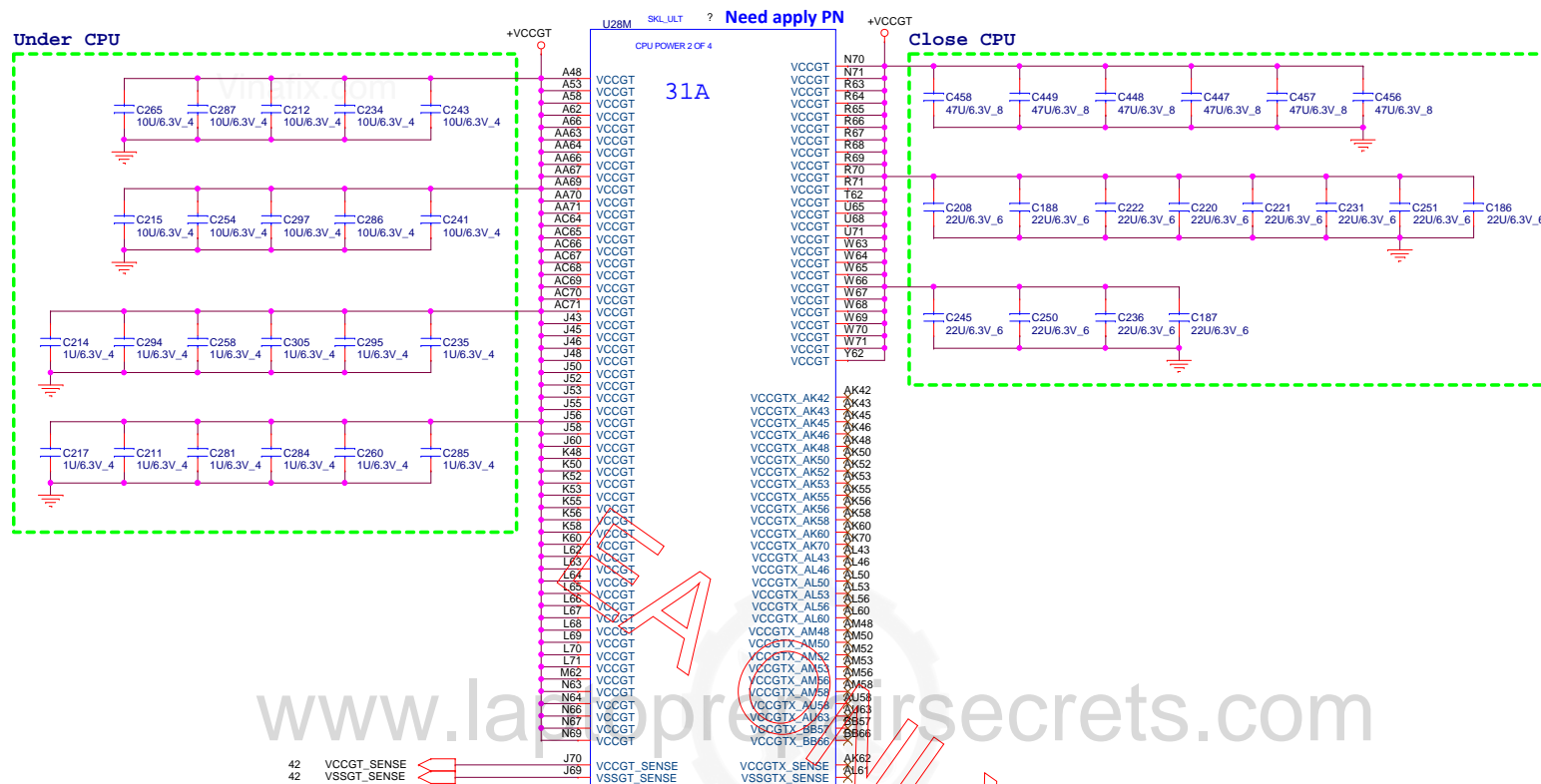
SVID DATA

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Size	Document Number Custom 05 – SKYPAKE 6/20 (POWER-1)	Rev 1A
Date:	Monday, November 09, 2015	Sheet 5 of 57

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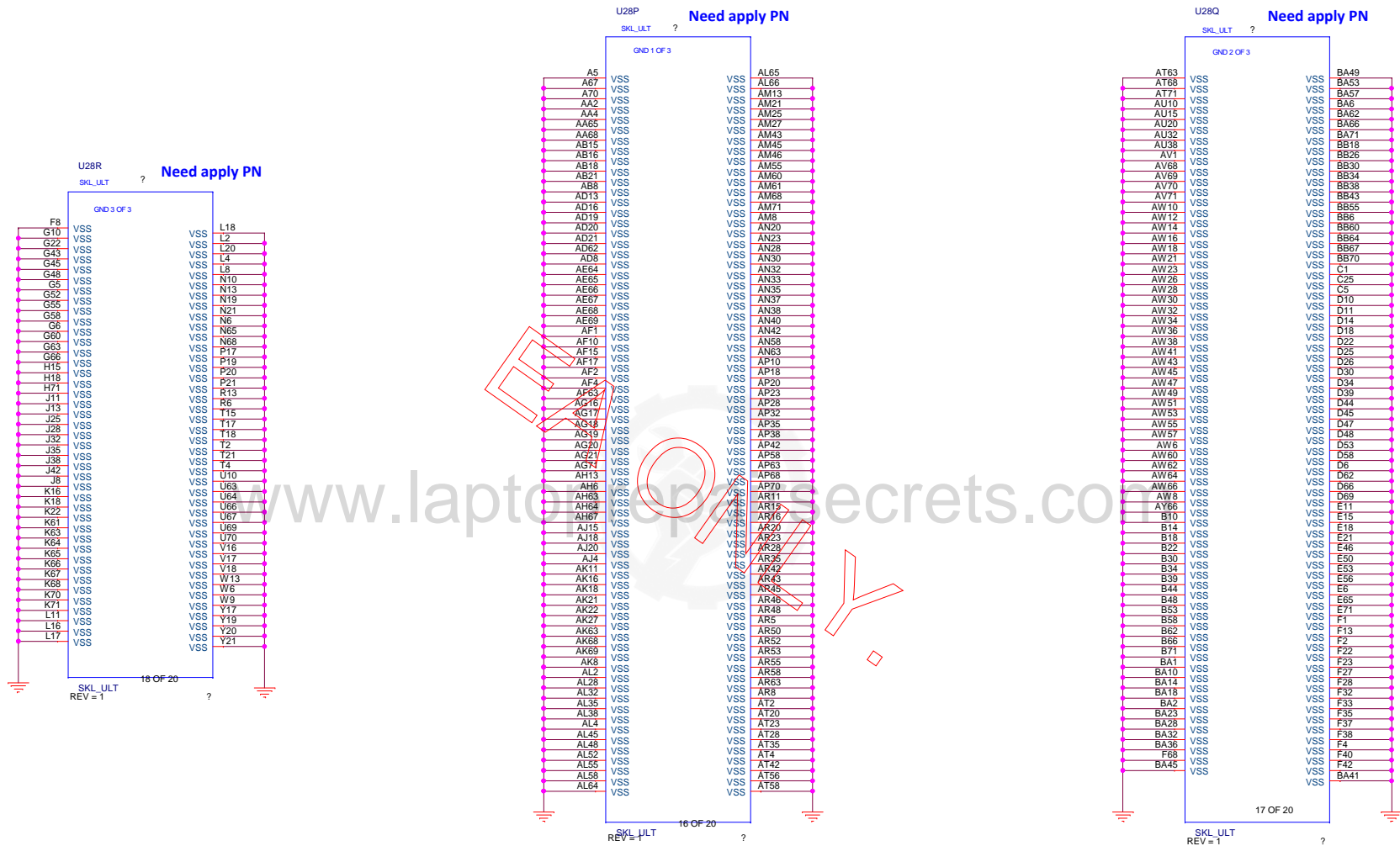


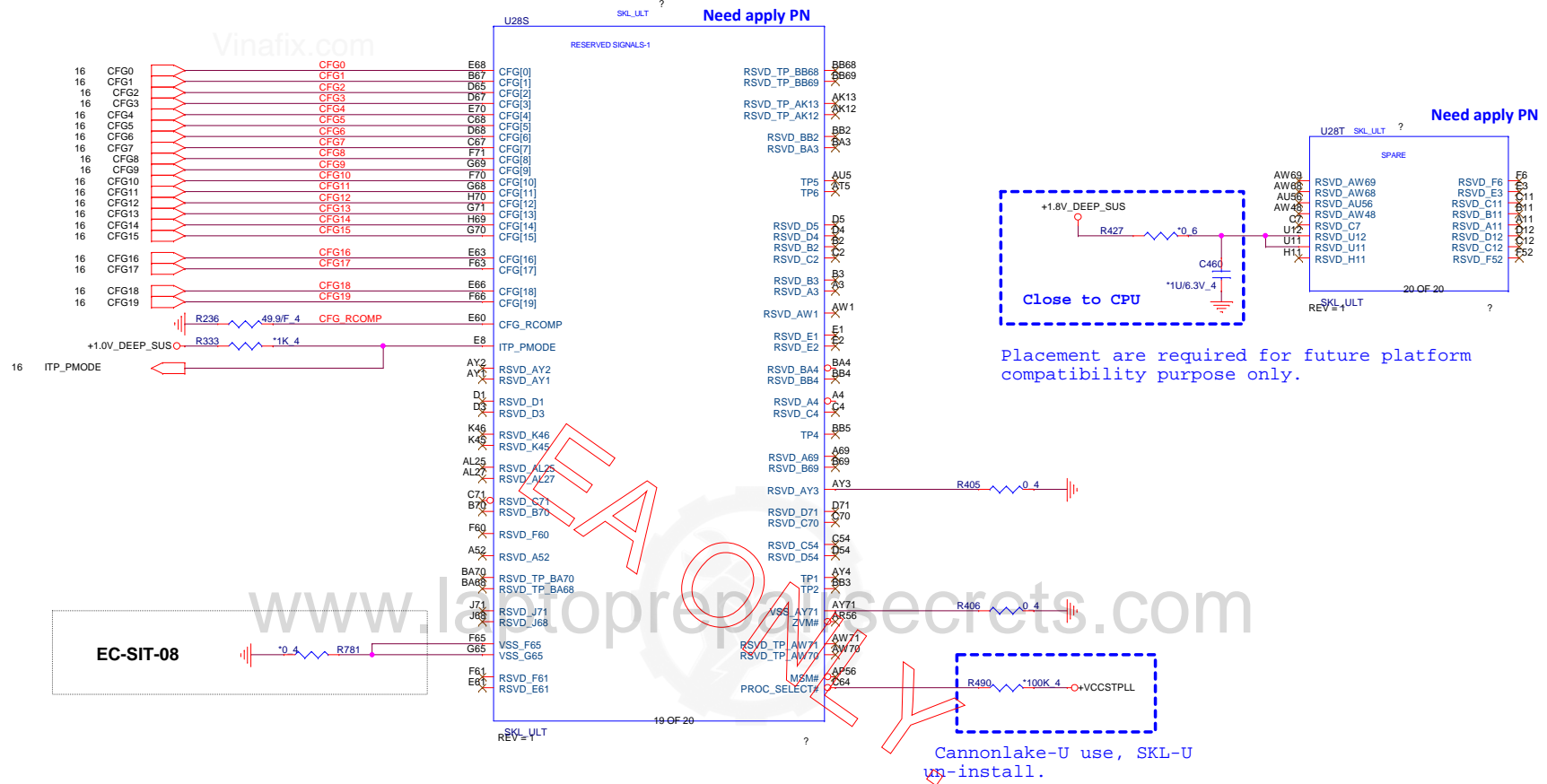
Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGT} TX	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCIOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed



Power Rail	Description	Control
V _{CC}	Processor IA Cores Power Rail	SVID
V _{CCGT}	Processor Graphics Power Rails	SVID
V _{CCGTx}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
V _{CCSA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
V _{CCIO}	IO Power Rail	Fixed
V _{CCST}	Sustain Power Rail	Fixed
V _{CCPLL}	Processor PLLs power rail	Fixed
V _{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
V _{CCOPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCOPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
V _{CCEOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

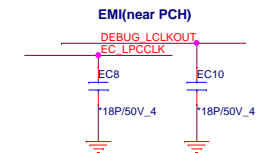
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Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physical Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R440 *1K 4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R439 1K 4

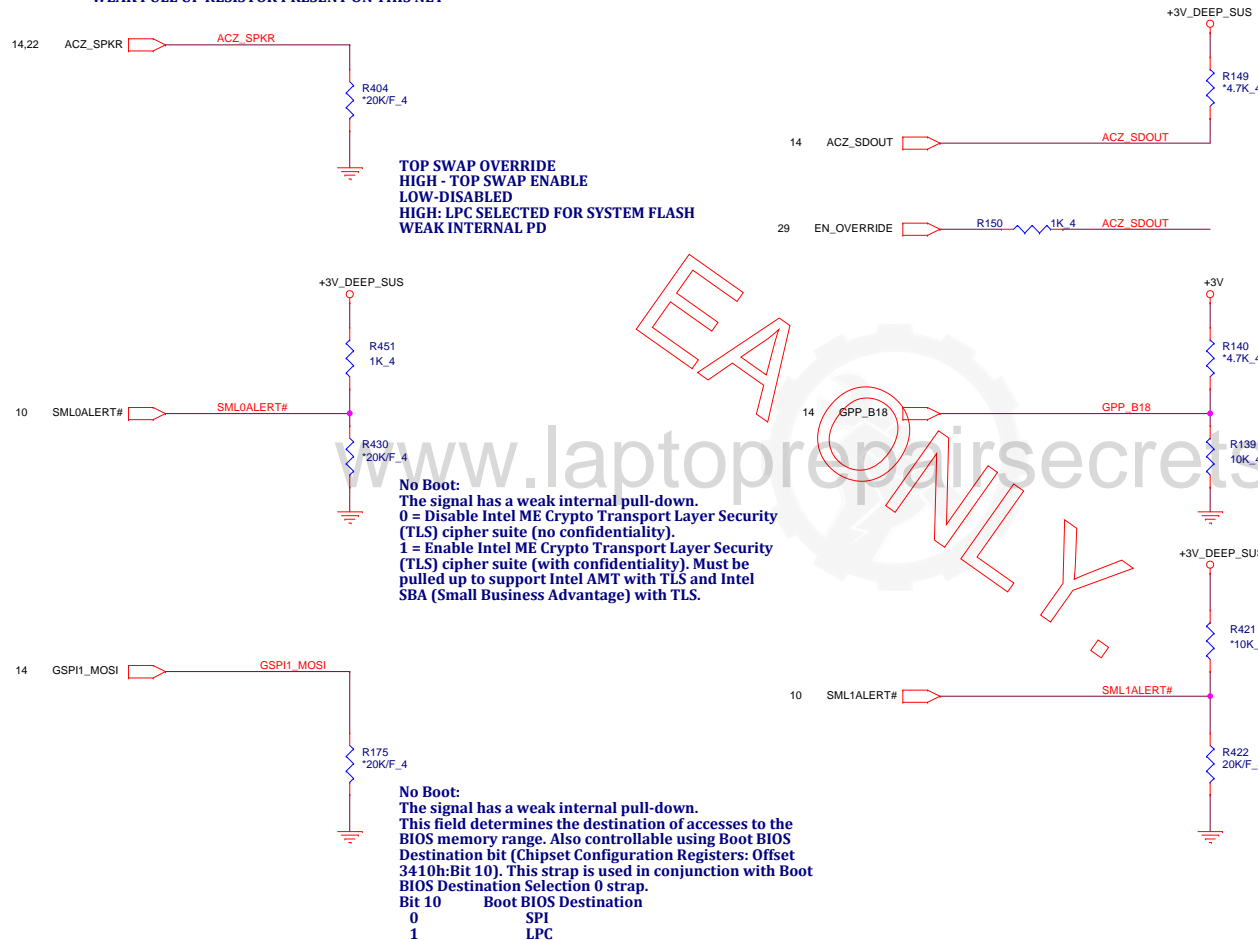


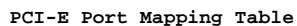
TP15	PCB SPI_CS0#_R	PCB_SPI_CS0#_R	29
TP9	PCB SPI1_CLK_R	PCB_SPI1_CLK_R	29
TP12	PCB SPI1_SI_R	PCB_SPI1_SI_R	29
TP13	PCB SPI1_SO_R	PCB_SPI1_SO_R	29
TP11	BIOS_WP#		
TP14	HOLD#		

Vender	Size	P/N
EON	16MB	AKE3DZNKQ00(EN25QH128AHIP)
Winbond	16MB	AKE3DZN0N01 (W25Q128FVSIQ)
Socket		DFHS08FS023

Functional Strap Definitions

DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET





PCI-E Port	Function	CLK RQ Port	Function
Port1	Un-used	Port0	Un-used
Port2	Un-used	Port1	Un-used
Port3	Un-used	Port2	WLAN
Port4	WLAN	Port3	LAN
Port5	PCIESSD (Reseve)	Port4	SSD(Reserve)
Port6	PCIESSD (Reseve)	Port5	Un-used
Port7	PCIESSD (Reseve)		
Port8	HDD		
Port9	LAN		
Port10	Un-used		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	Onelink+
PORT-2	AOU5
PORT-3	USB HUB
PORT-4	USB TYPE-C

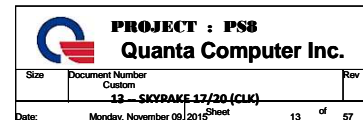
USB2.0 Port Mapping Table

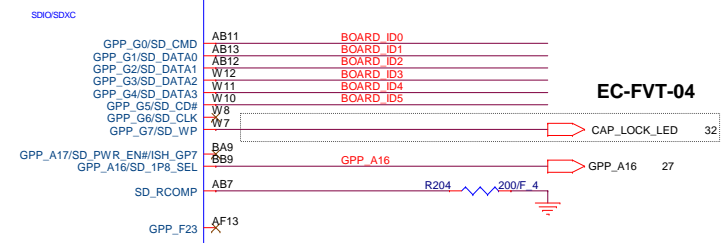
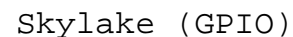
USB2.0	Function
PORT-1	AOU5
PORT-2	USB HUB
PORT-3	Camera
PORT-4	Cardreader
PORT-5	TYPE C
PORT-6	Onelink+
PORT-7	BT
PORT-8	FP
PORT-9	Touch Panel
PORT-10	NC

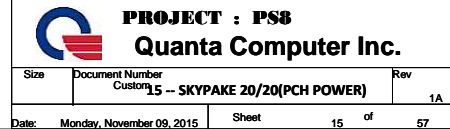


PROJECT : PS8
Quanta Computer Inc.

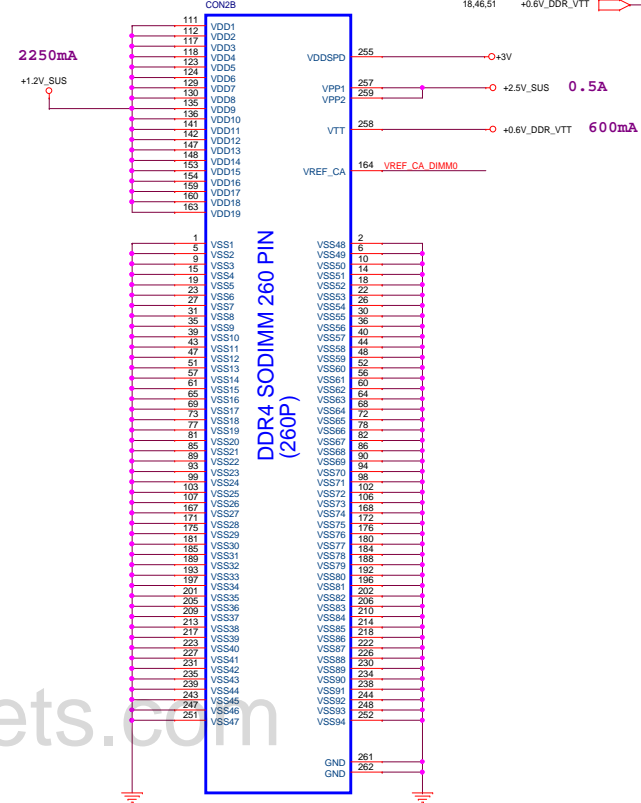
Size	Document Number Custom	Rev
	12 -- SKYPAKE 16/20 (PCIe/USB)	1/
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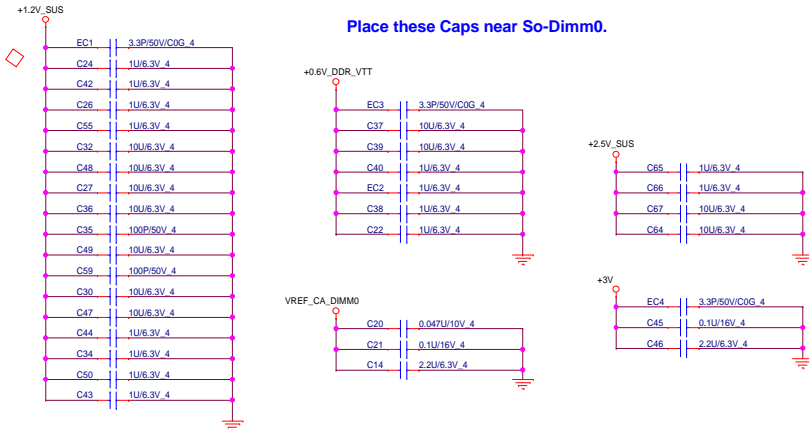


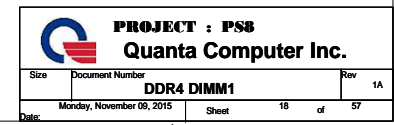




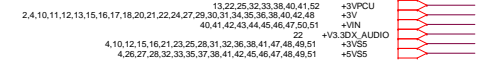
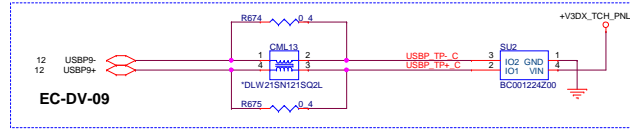
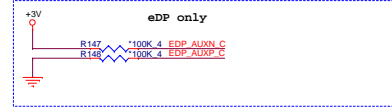
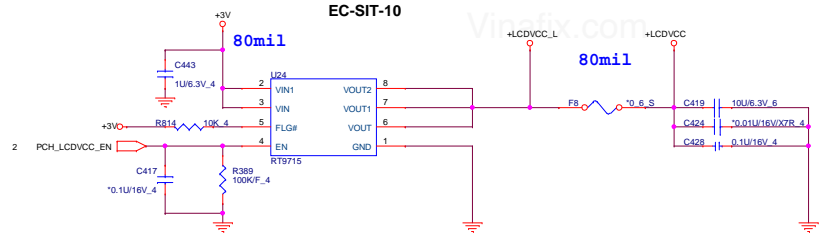


VREF CA DIMM0 Solution



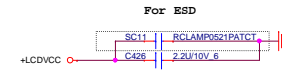
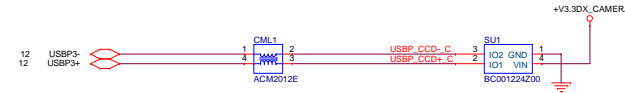
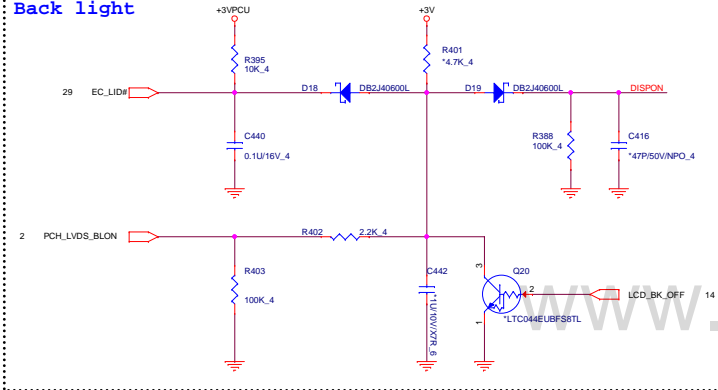


LCDVCC

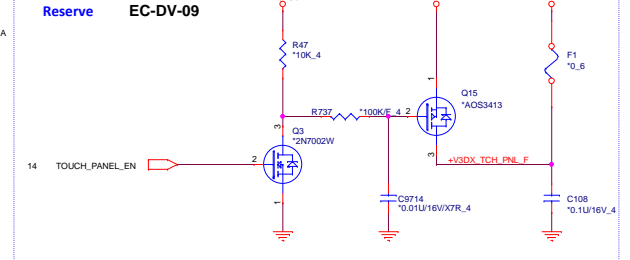


19

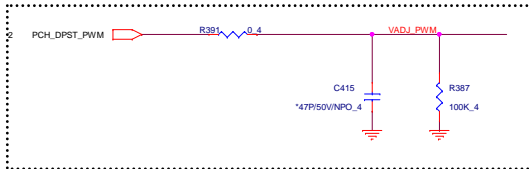
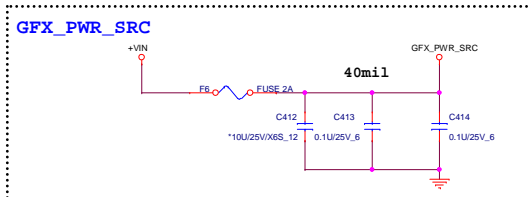
Back light



Touch Panel VCC Control



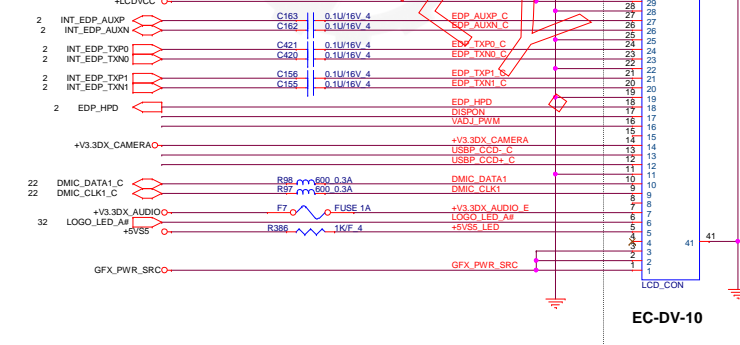
GFX_PWR_SRC



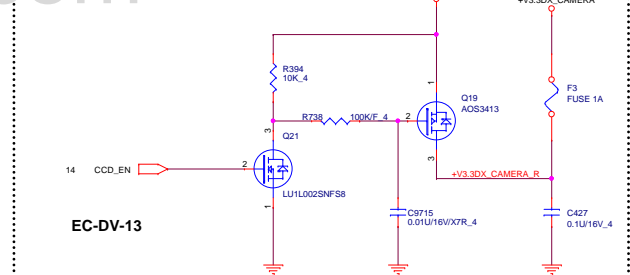
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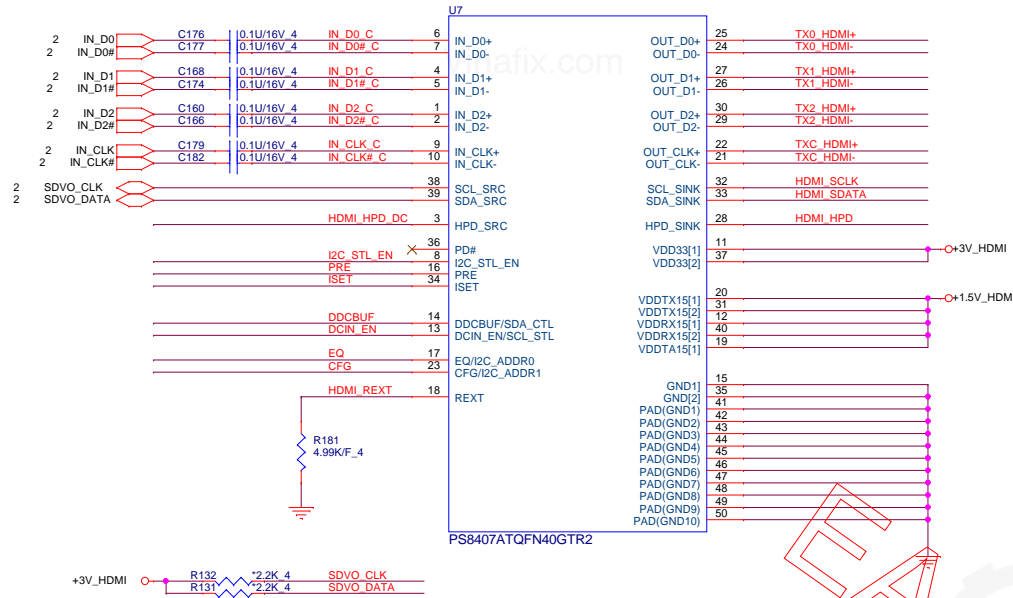
Touch Panel

EC-SIT-14

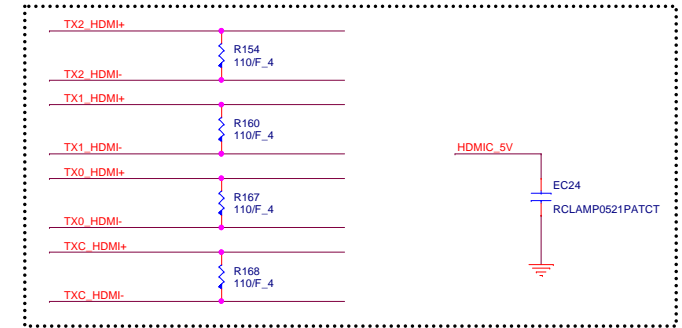


CAMERA VCC Control

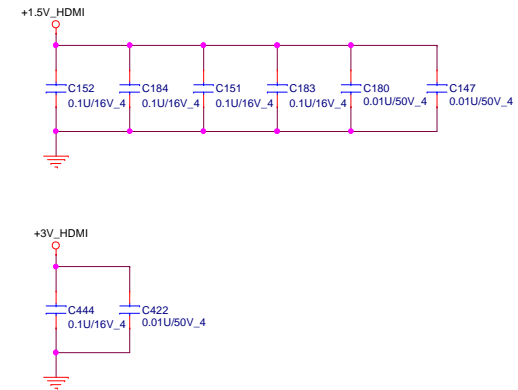
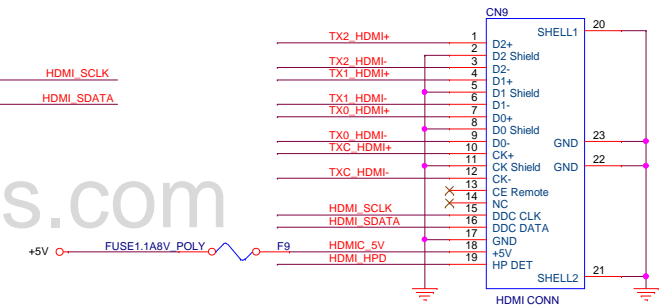
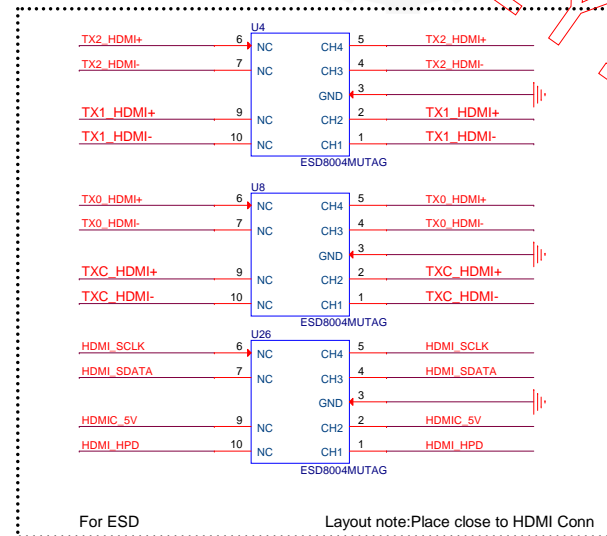
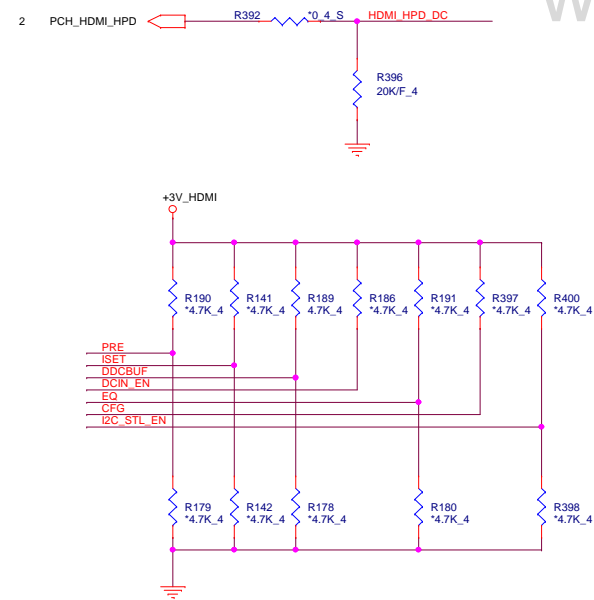
+CAM_VCC
Max Current : 800mA



EMI reserve for HDMI



HDMI HPD SENSE



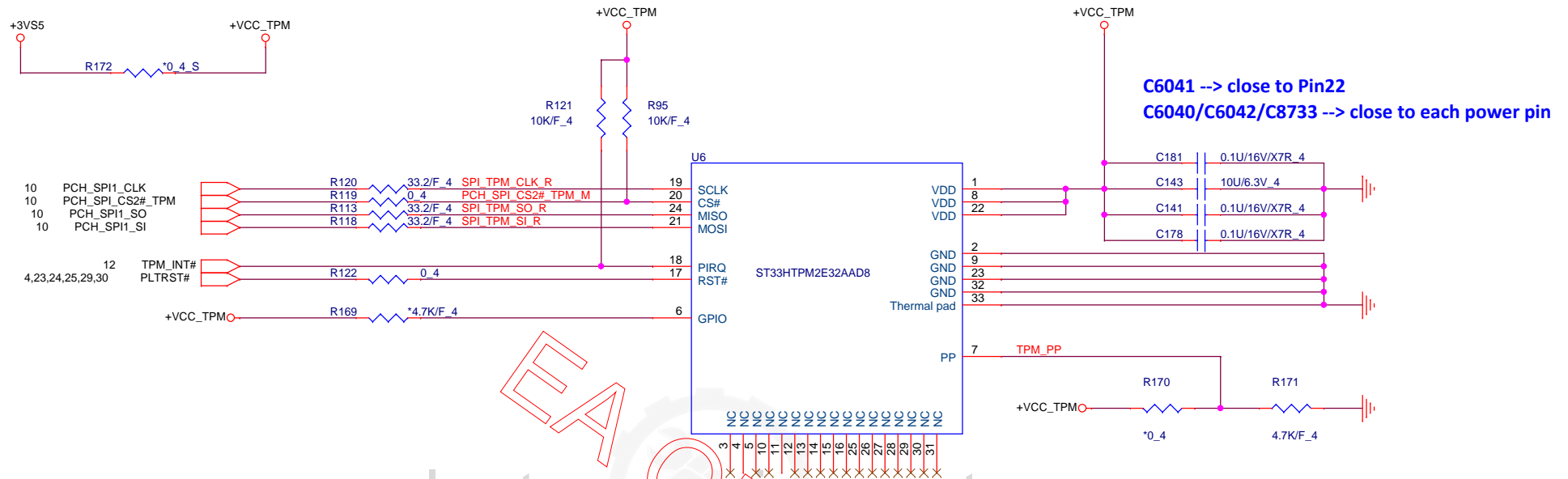
TPM

2nd source: AL33HTPM000

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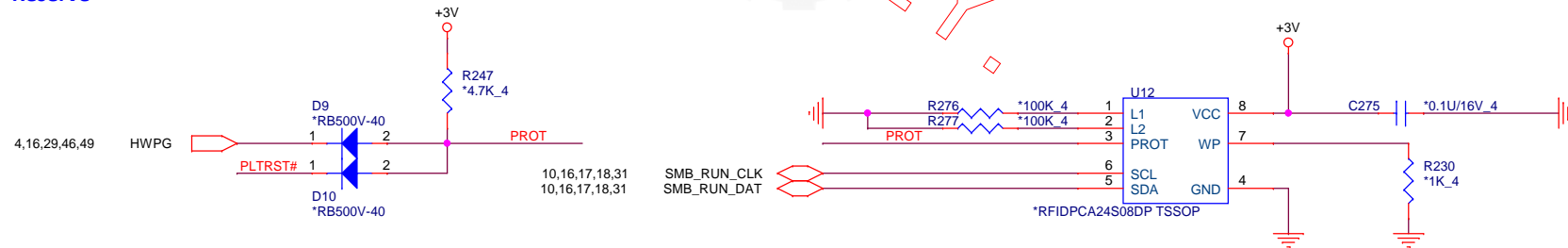
+3V
+3VS5

21



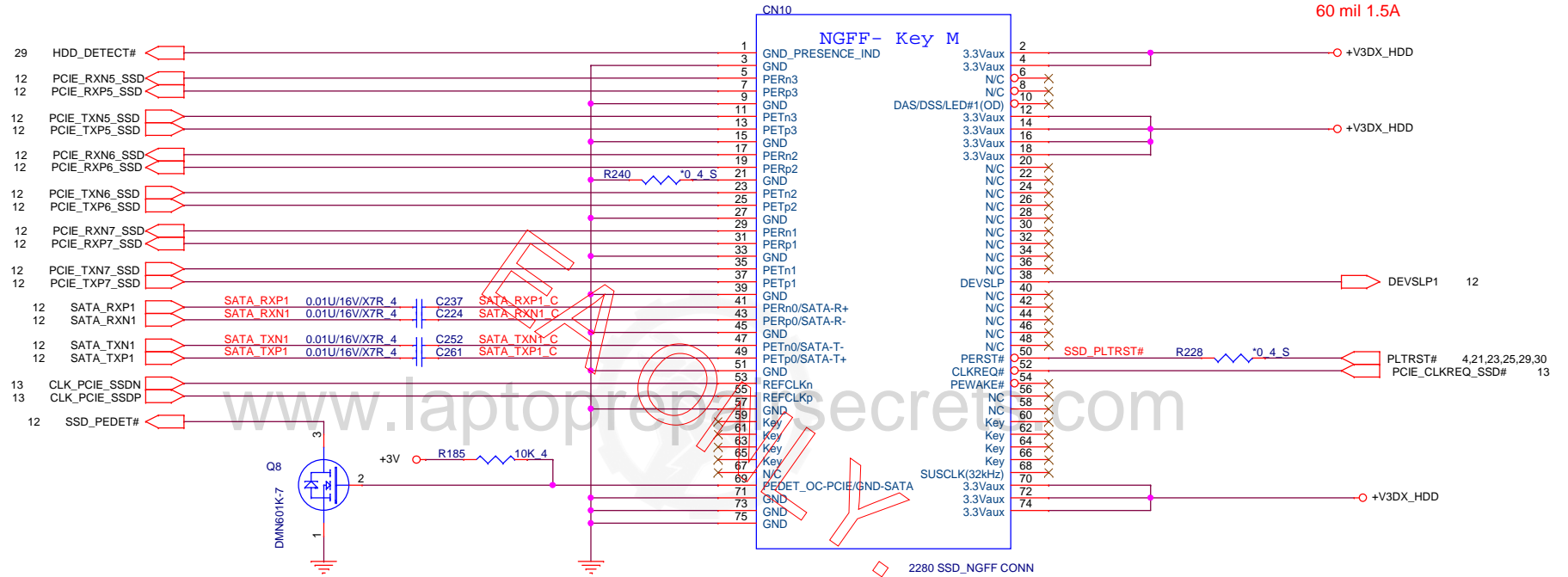
RFID

Reserve

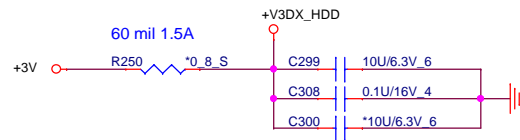


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		Quanta Computer Inc.	
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	TPM/RFID	1A	
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DC Current rating: 3 A (MAX)



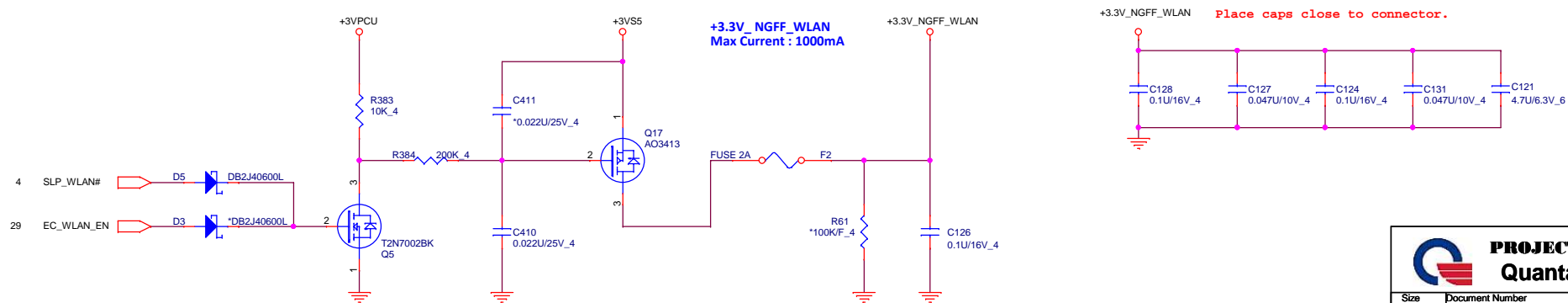
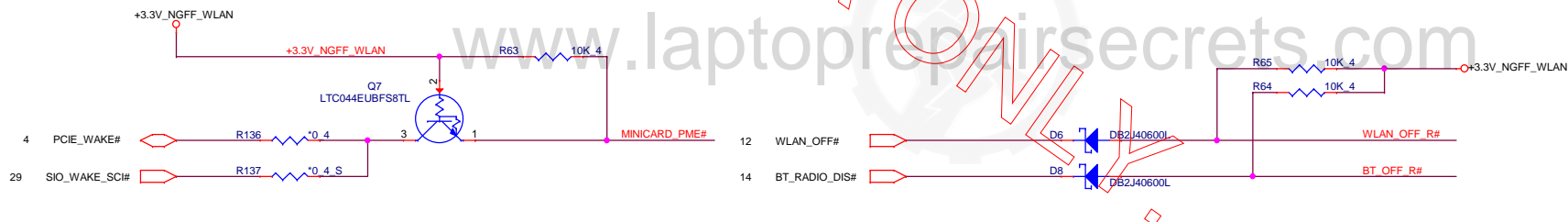
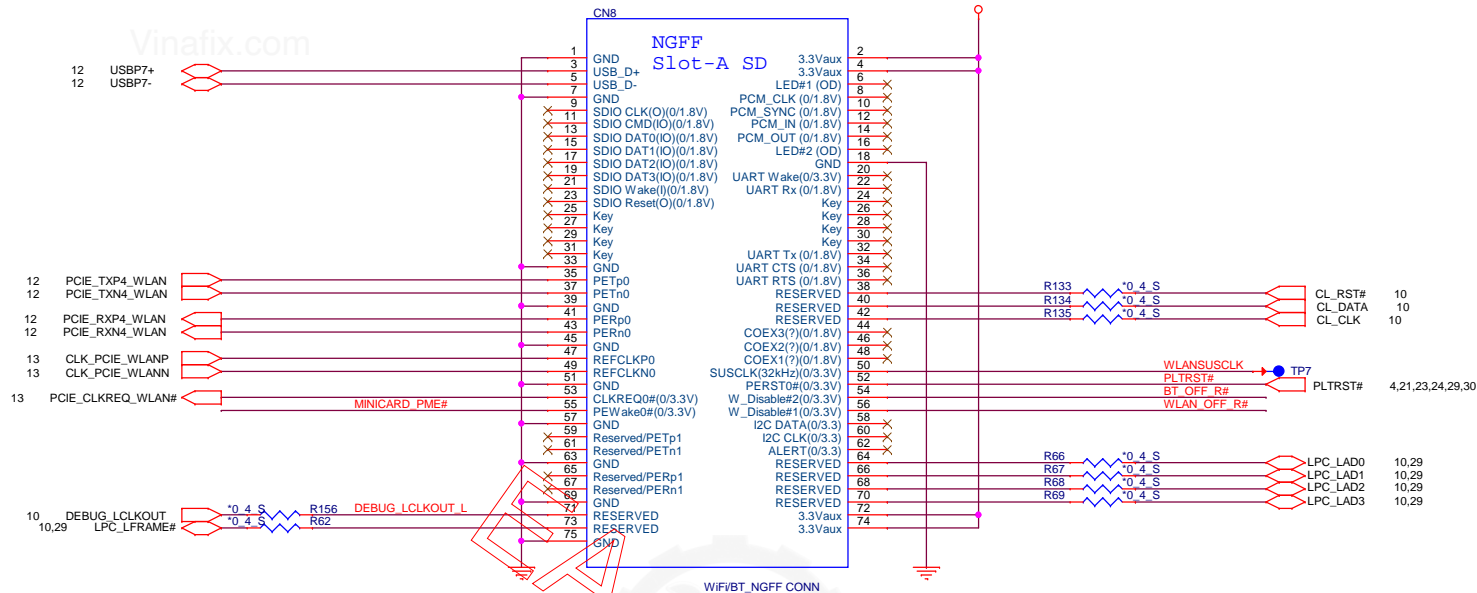
PROJECT : PS8
Quanta Computer Inc.


Size	Document Number	Rev
	SATA/G-sensor	1A
Date:	Monday, November 09, 2015	Sheet 24 of 57

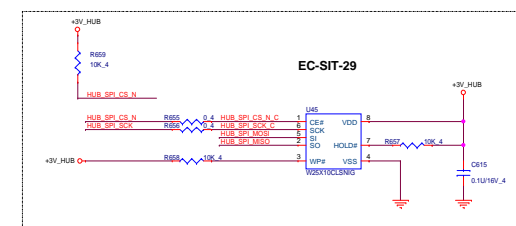
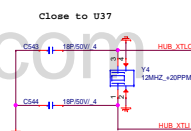
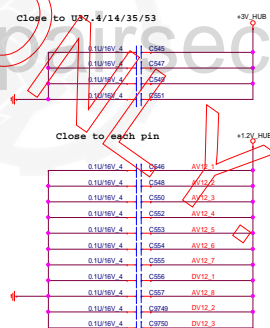
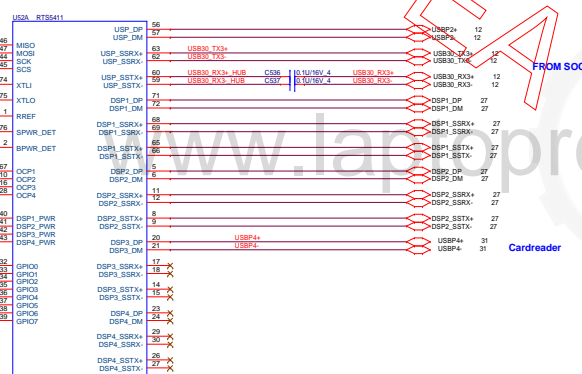
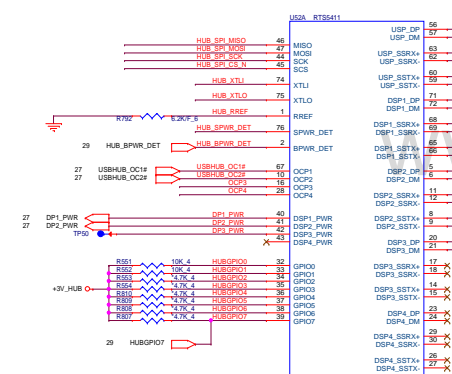
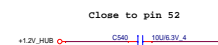
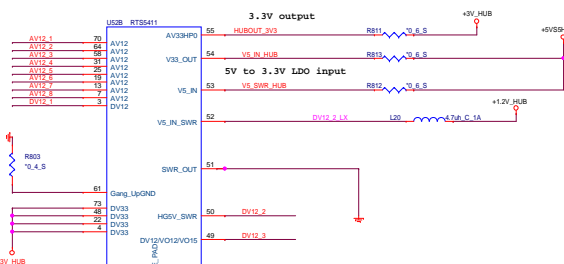
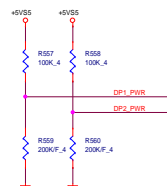
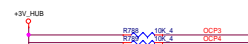
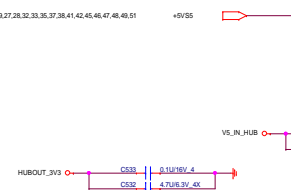
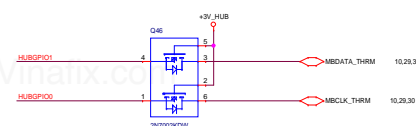
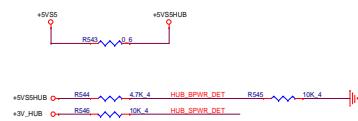
NGFF WiFi/BT connector
M.2 2230


4,10,12,15,16,19,21,23,28,31,32,36,38,41,47,48,49,51 +3VS5
13,19,22,32,33,38,40,41,52 +3VPCU

25

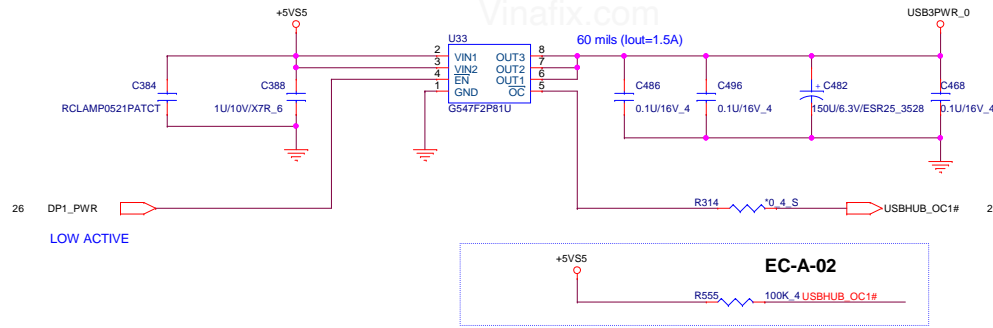


	PROJECT : PS8 Quanta Computer Inc.	
	Size _____ Document Number _____ Wifi/BT NGFF	Rev _____ 1A
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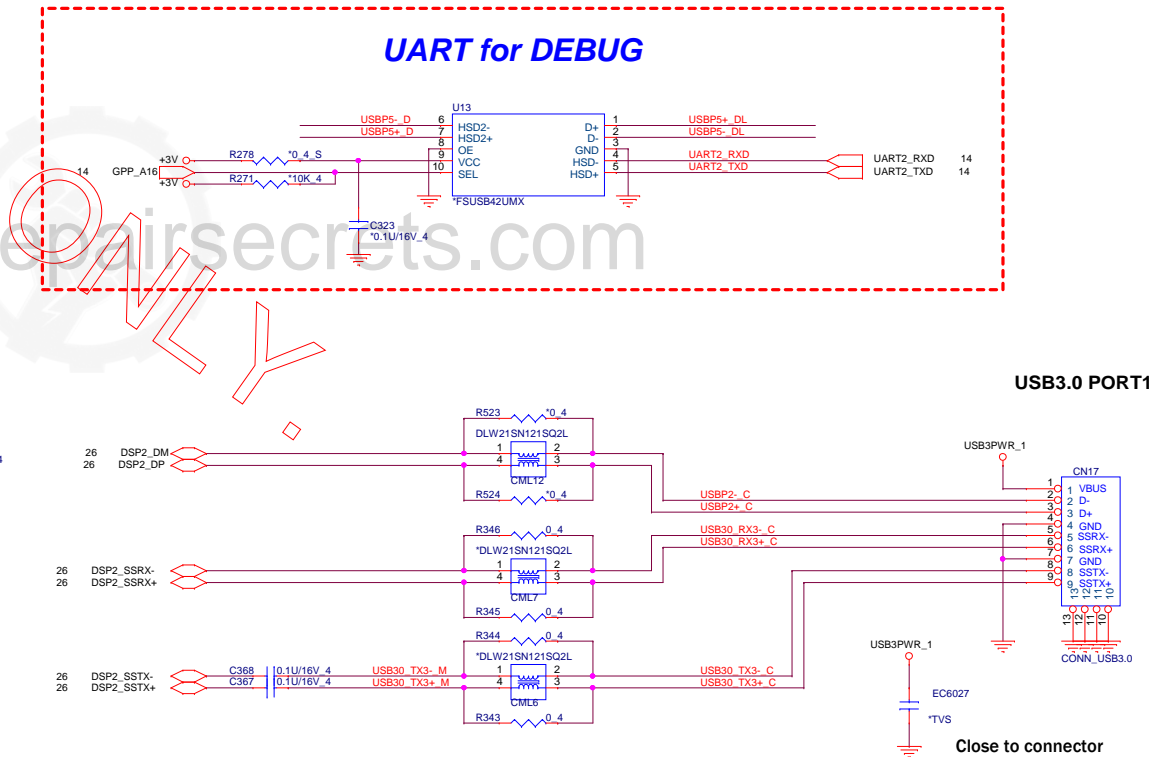
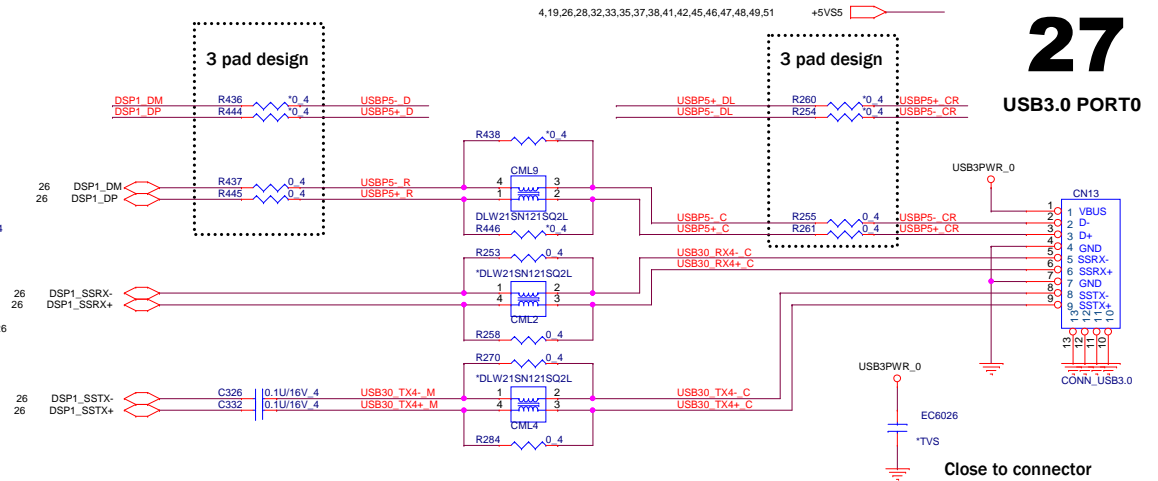
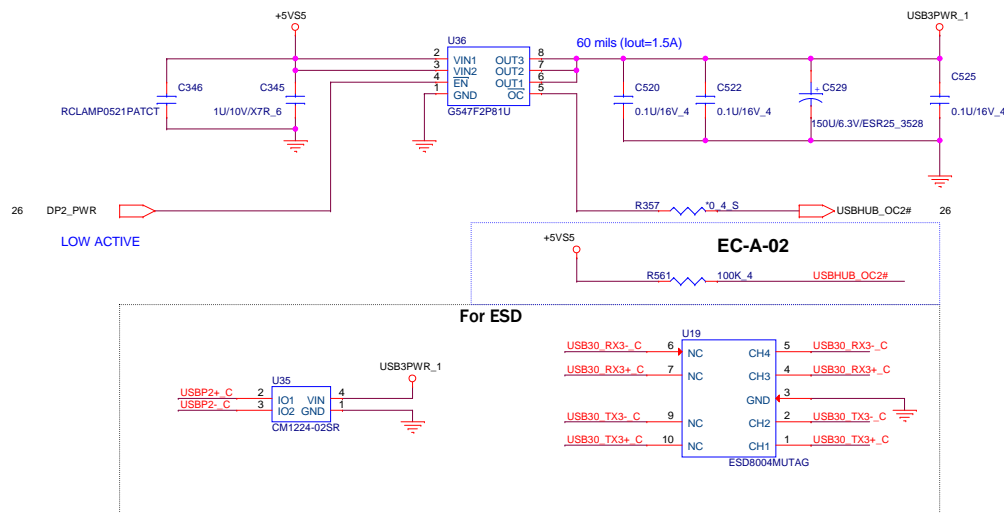


 PROJECT : PSB Quanta Computer Inc.		
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Custom	USB HUB	1
Date	Monday, November 20, 2006	Sheet 1 of 1

USB 3.0 Port L-side



USB 3.0 Port R-side



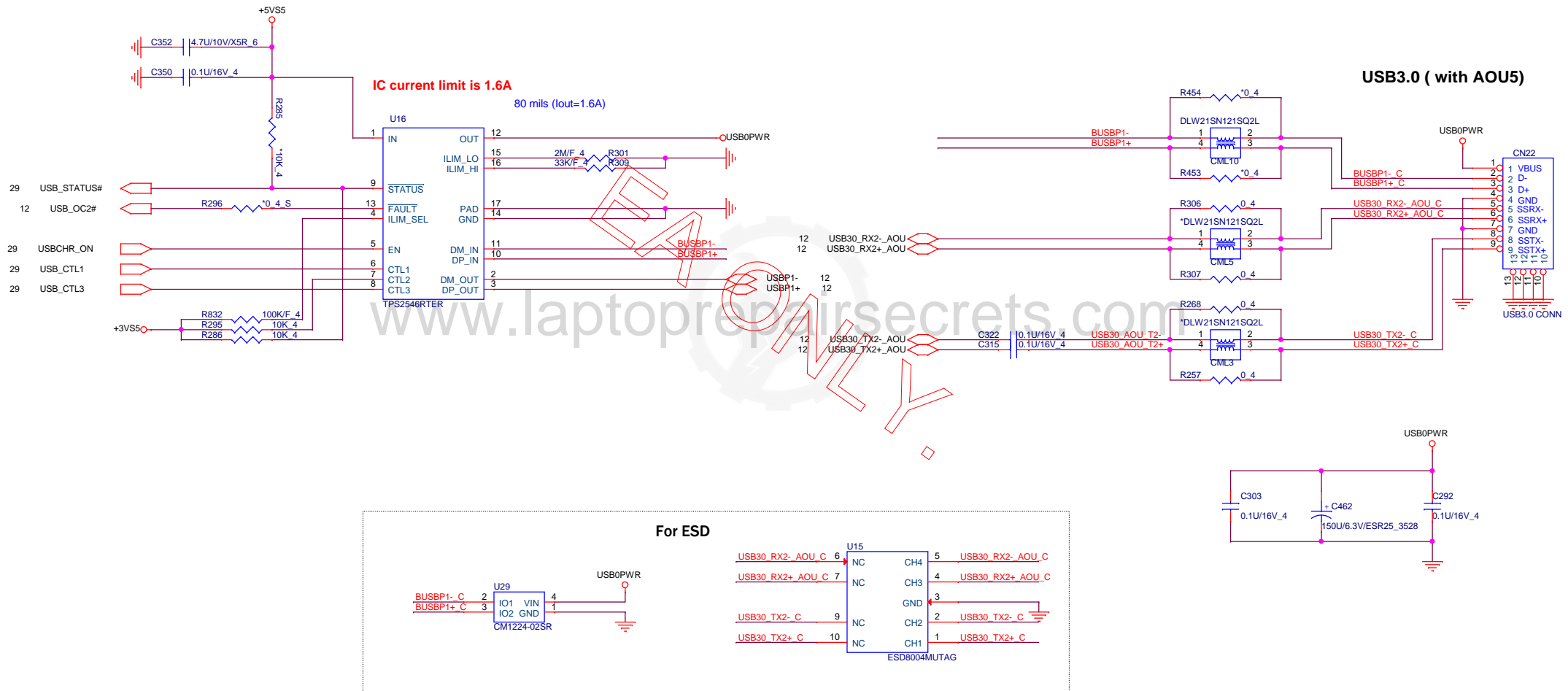
USB 3.0 Port (AOU5)

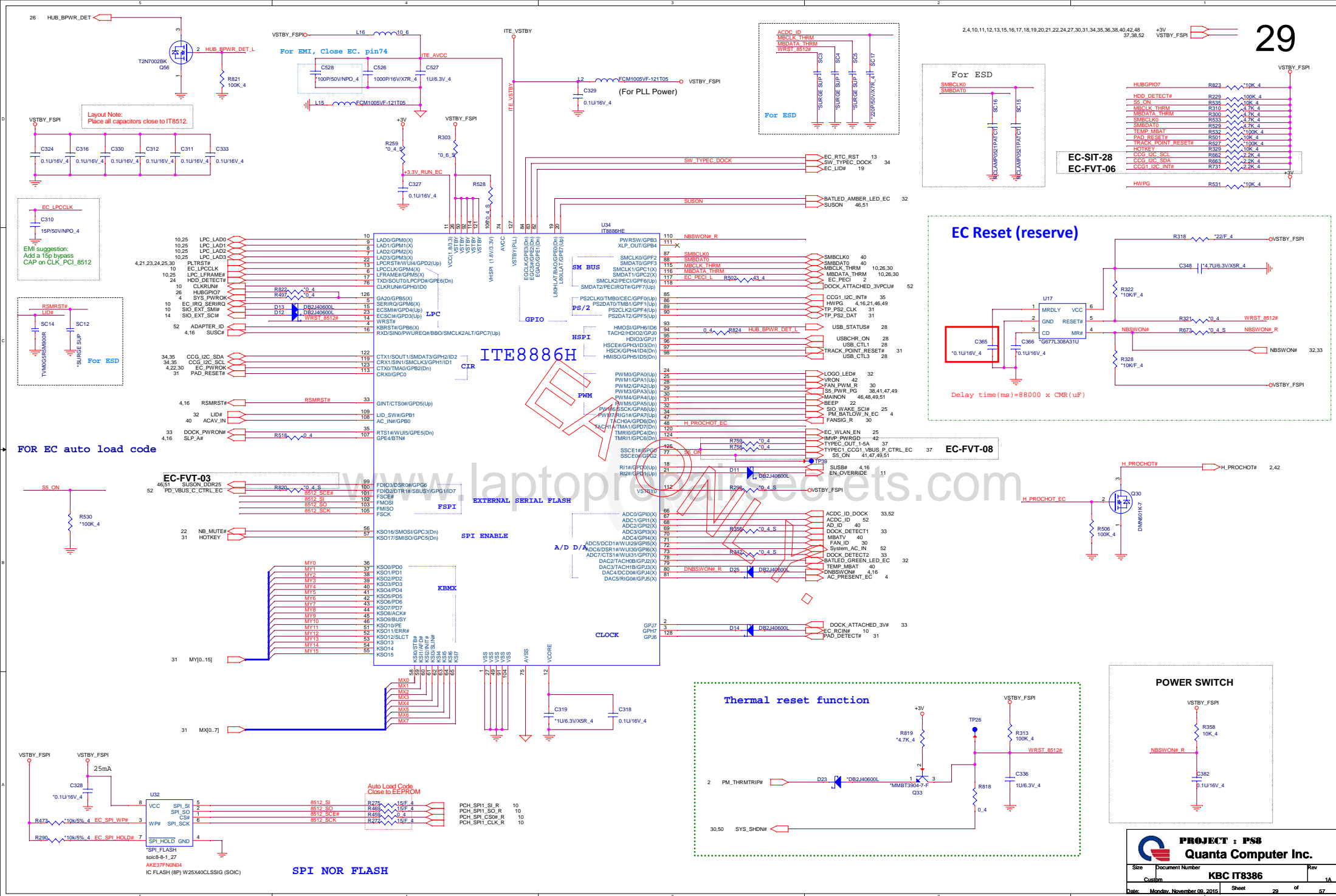
Vinafix.com

4, 19, 26, 27, 32, 33, 35, 37, 38, 41, 42, 45, 46, 47, 48, 49, 51
4, 10, 12, 15, 16, 19, 21, 23, 25, 31, 32, 36, 38, 41, 47, 48, 49, 51

+5VS5
+3VS5

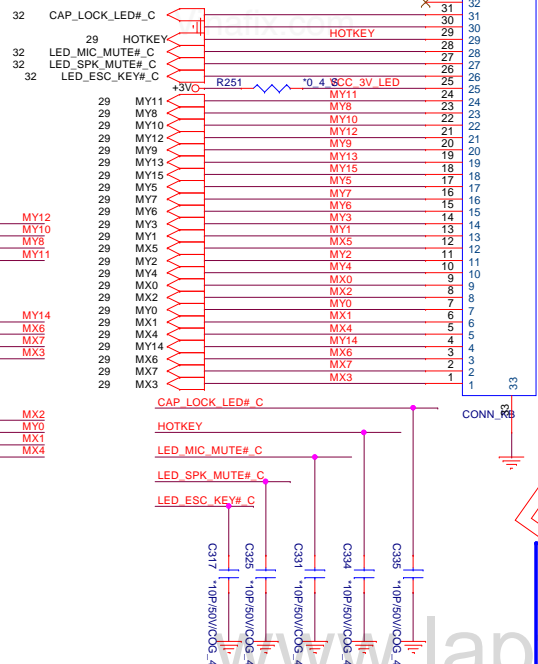
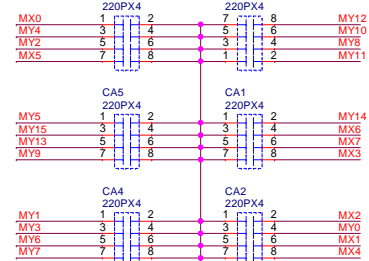
28





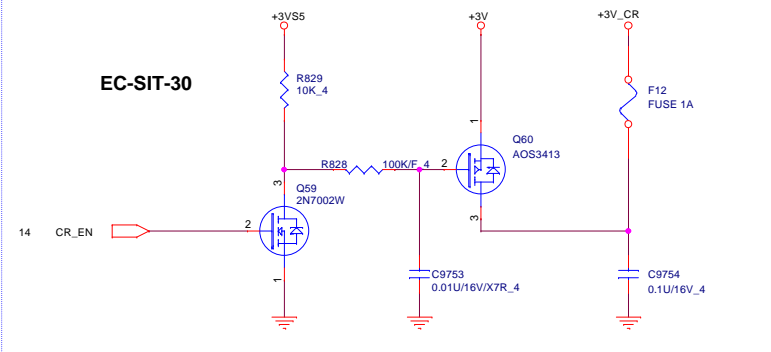
KEYBOARD

For EMI request



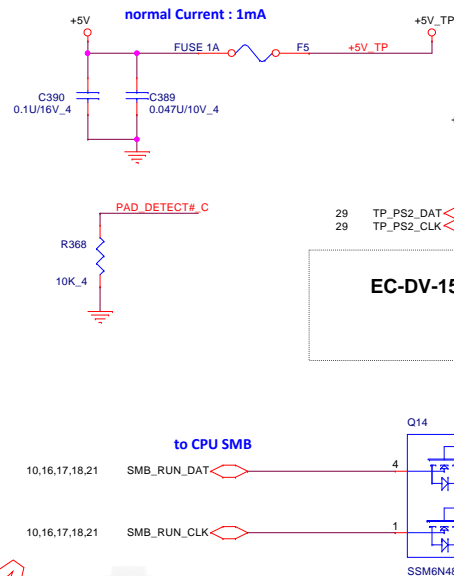
CR VCC Control

EC-SIT-30

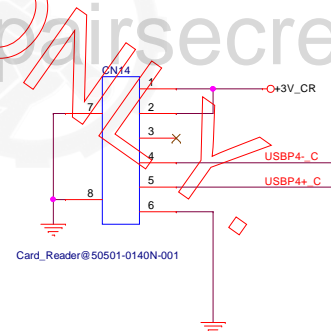


TP Control

normal Current : 1mA



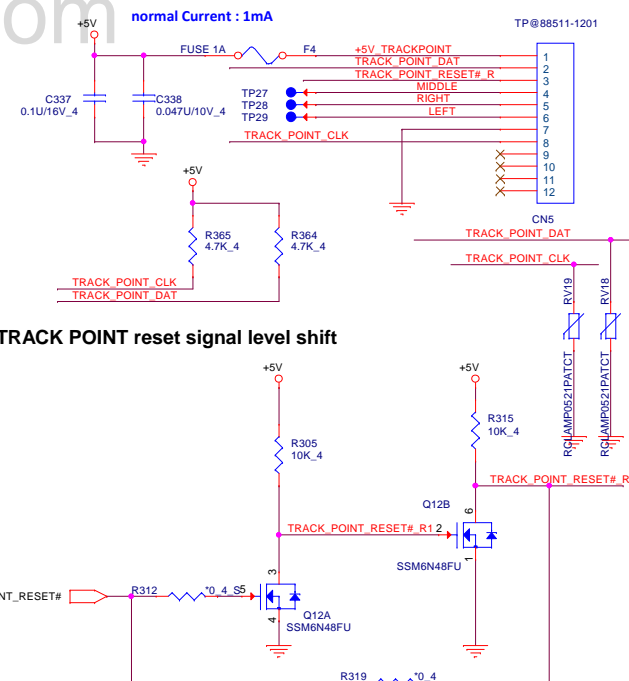
To Card Reader Board



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	KB/TP/DB	1A
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Track point

normal Current : 1mA



TRACK POINT reset signal level shift

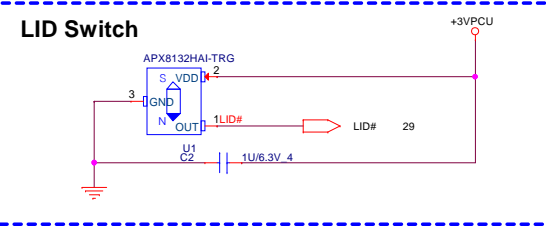
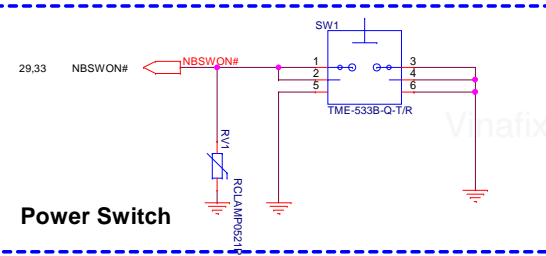
29

31

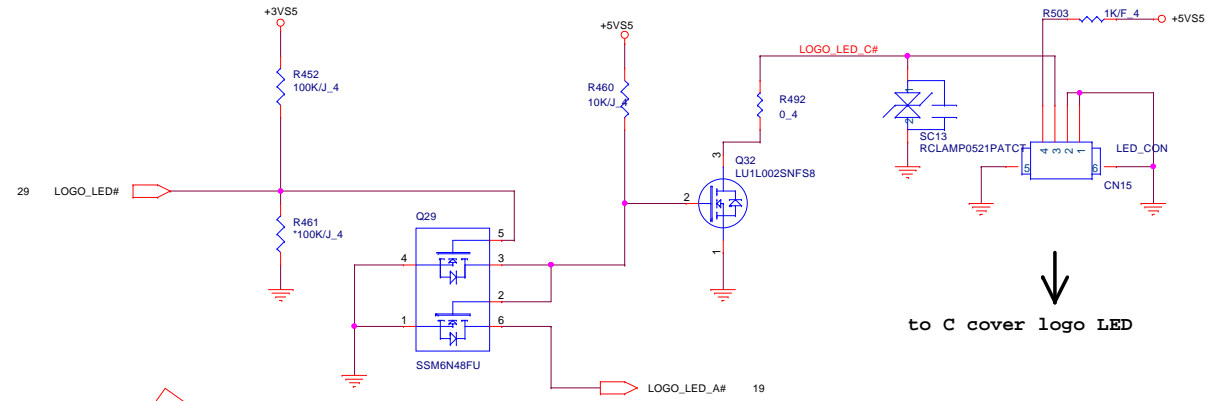
Touch pad

TP@88511-1201



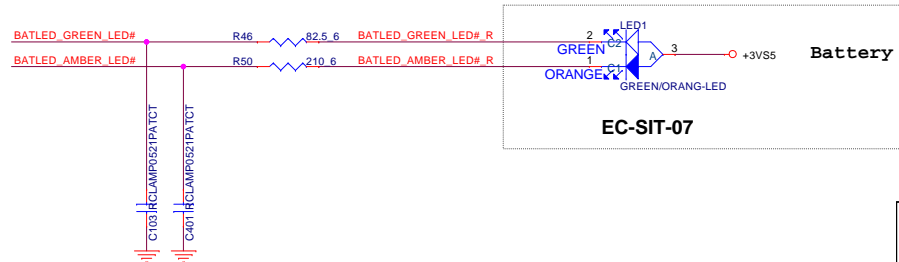
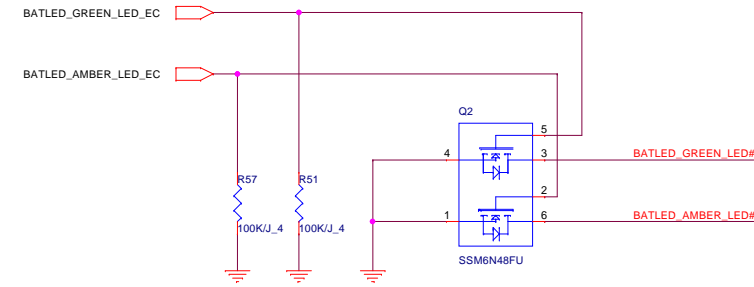
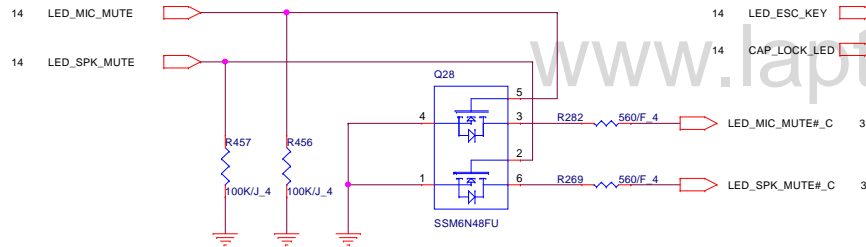
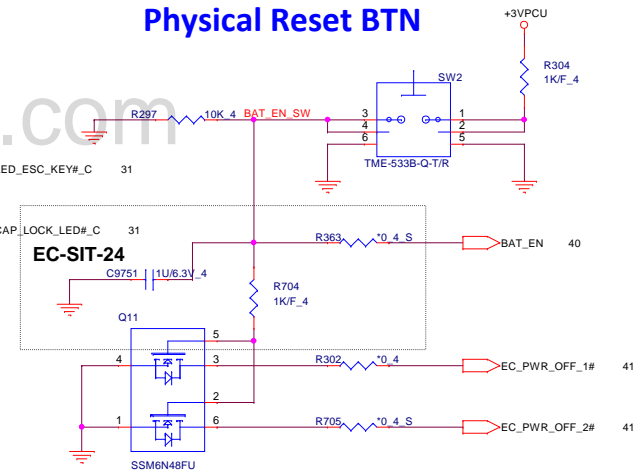


LED Driver

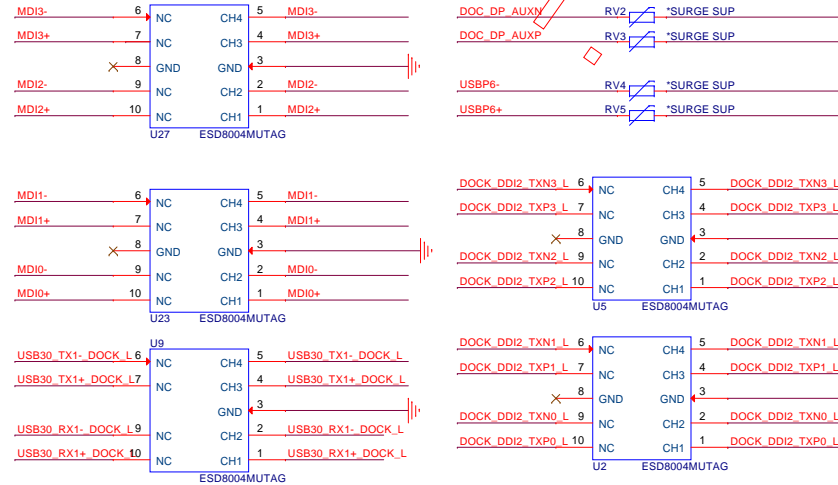
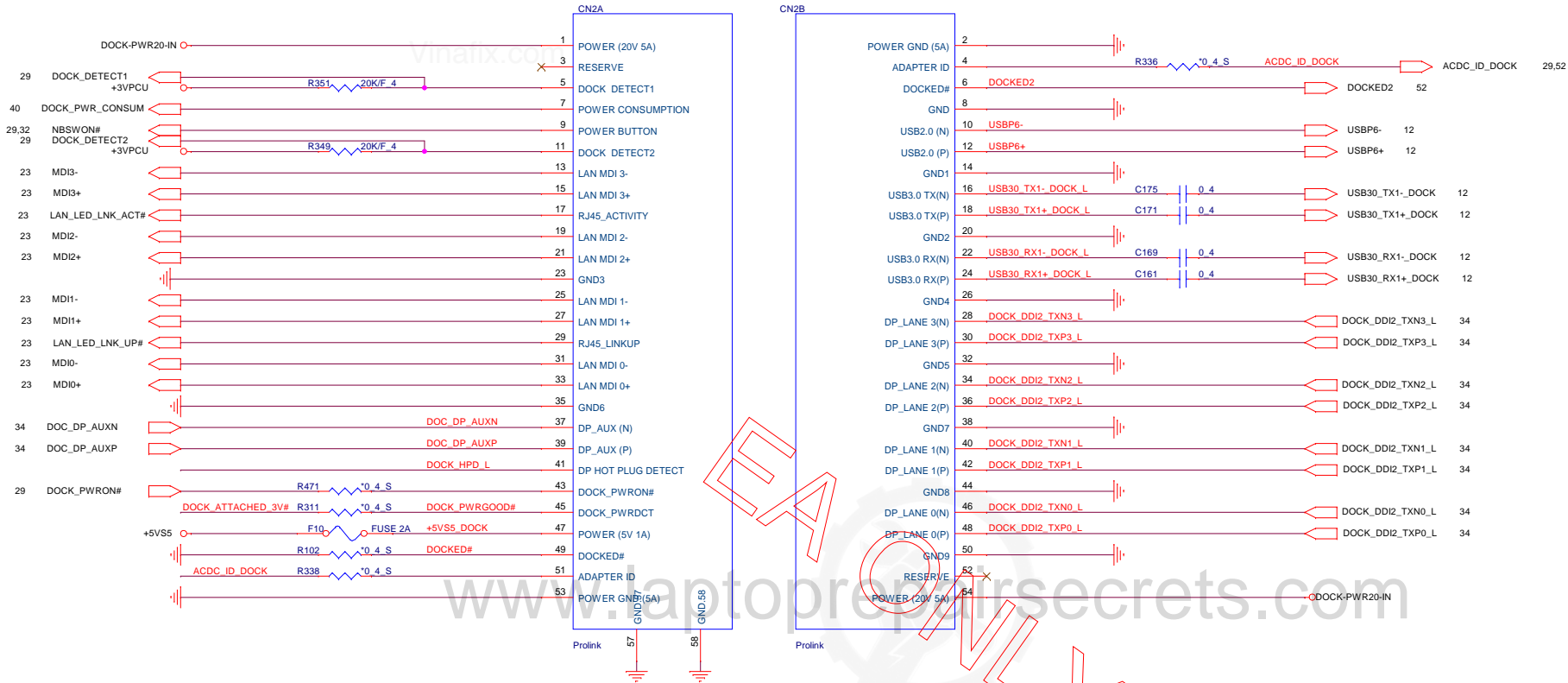


to C cover logo LED

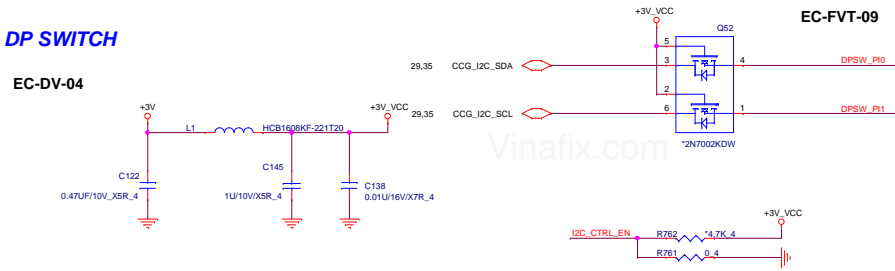
Physical Reset BTN



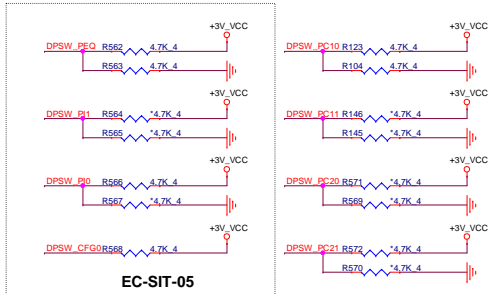
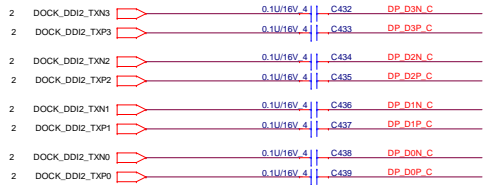
13,19,22,25,32,38,40,41,52
20,22,30,31,40,48
+3VPCU
+5V
+3V
+5VSS
DOCK-PWR20-IN



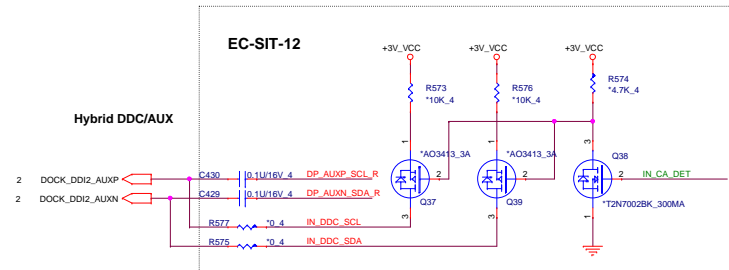
EC-DV-01



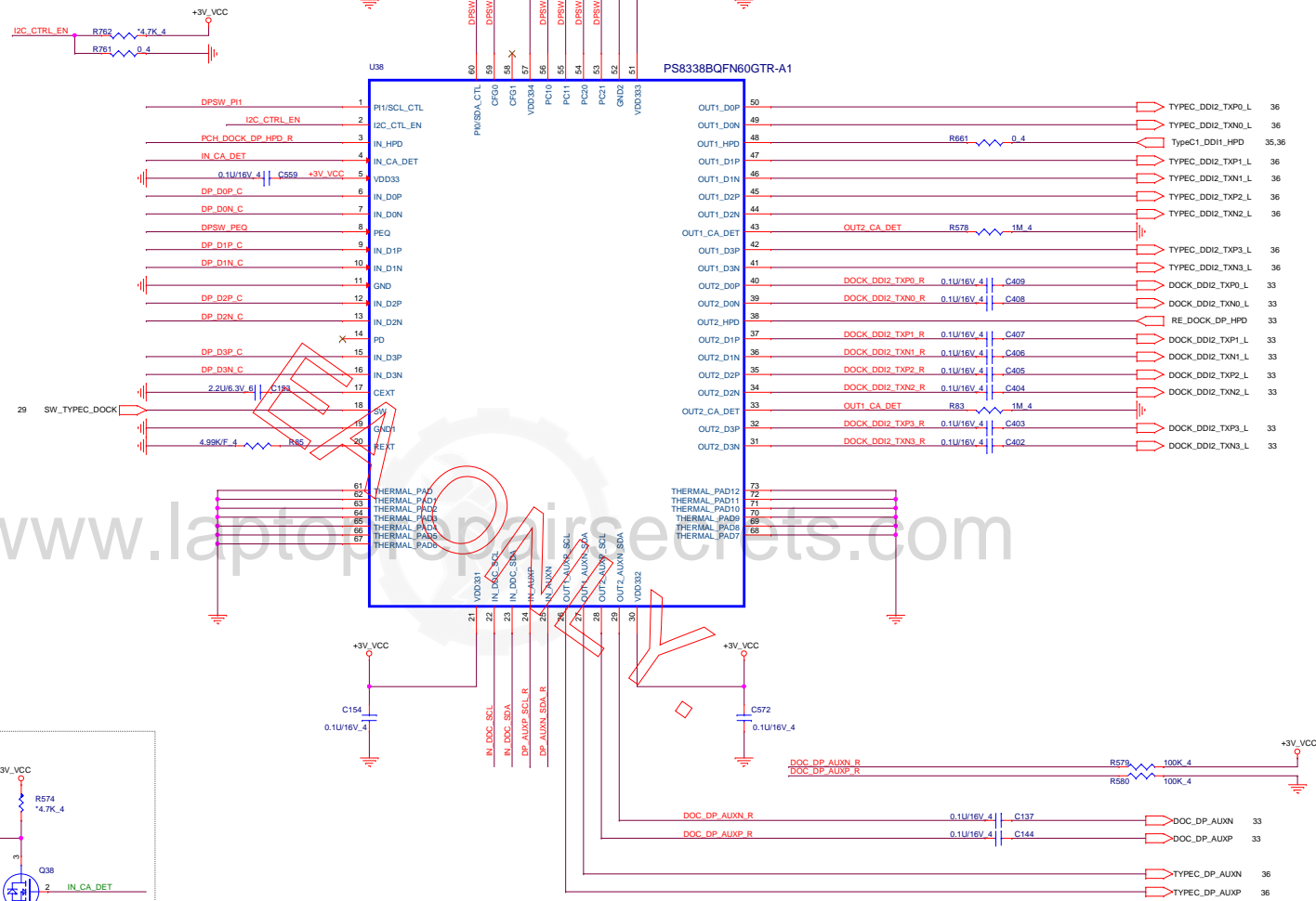
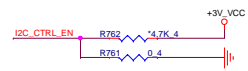
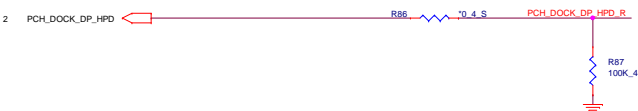
From CPU side



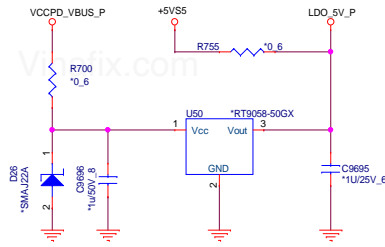
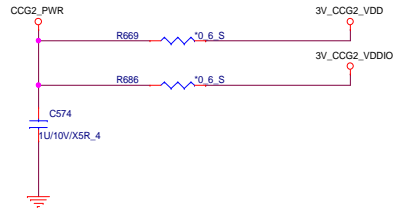
EC-SIT-12



Hybrid DDC/AUX



SW_TYPEC_DOCK	Display Priority
Low	USB Type-C
High	Docking Station

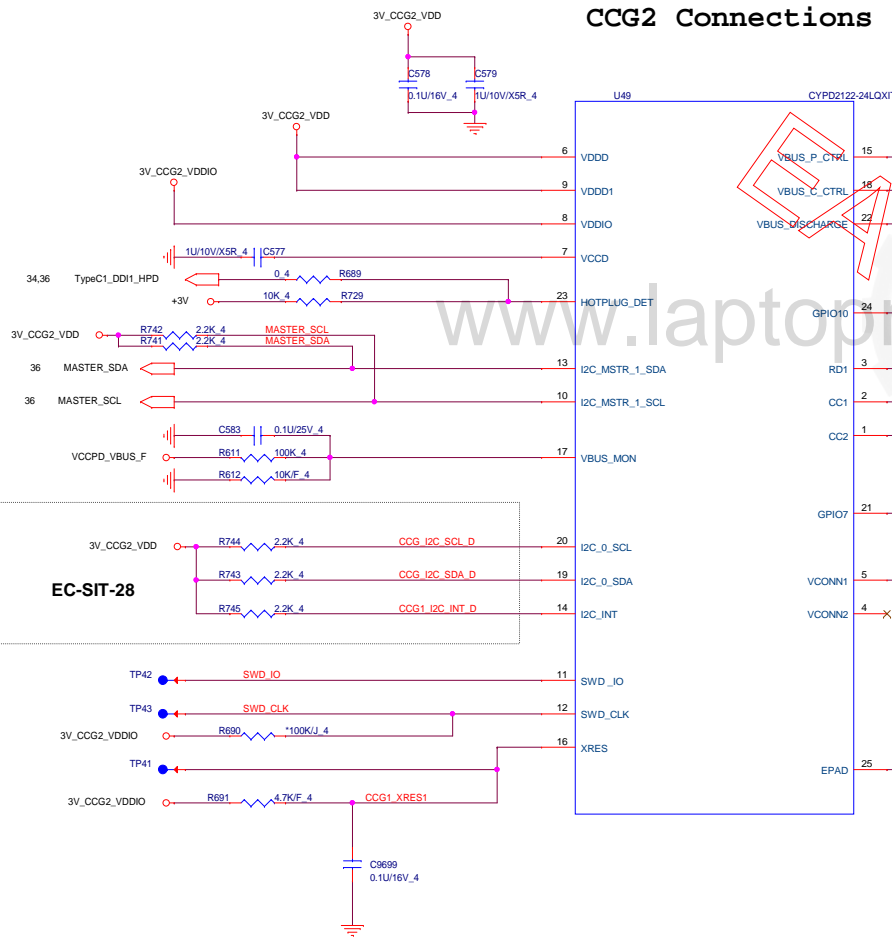


4,19,26,27,28,32,33,37,38,41,42,45,46,47,48,49,51
4,10,12,15,16,19,21,23,25,28,31,32,36,38,41,47,48,49,51
52
38,40,52

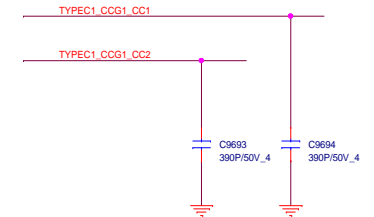
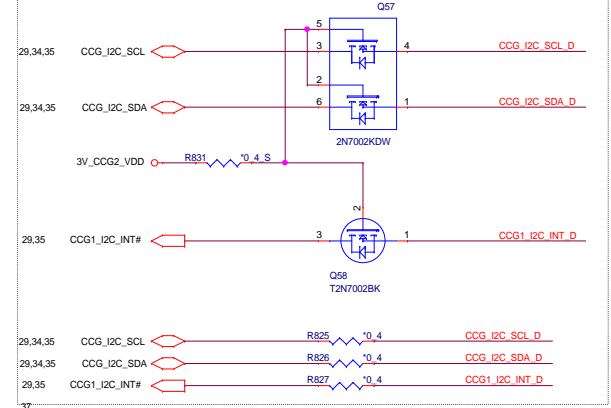
+5VS5
+3VS5
VCCPD_VBUS_P
VCCPD_VBUS_F

EC-SDV-07

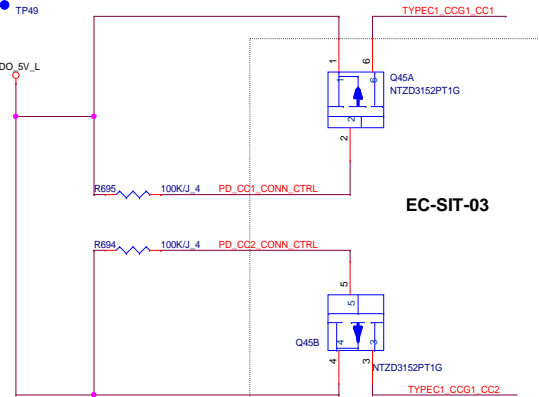
CCG2 Connections



EC-SIT-28



EC-SIT-03



EC-DV-05

3 Level Input:
L: LOW, internal pull down
H: HIGH, external pull up
M: VDD33/2, both external pull-up and pull-down

4,10,12,15,16,19,21,23,25,28,31,32,38,41,47,48,49,51

+3VS5
+3V_VCC

USB Type-C connector facing TX channel
De-emphasis setting; Internal tied to VDD33/2, 3.3V I/O.
CDE =
L: Programmable DE level#1
H: Programmable DE level#2
M: Programmable DE level#3 (default)

USB Type-C connector facing RX channel
receiver equalization setting; Internal tied to VDD33/2, 3.3V I/O.
CEQ =
L: Programmable EQ level#1
H: Programmable EQ level#2
M: Programmable EQ level#3 (default)

USB HOST facing TX channel
De-emphasis setting; Internal tied to VDD33/2, 3.3V I/O.
SSDE =
L: Programmable DE level#1
H: Programmable DE level#2
M: Programmable DE level#3 (default)

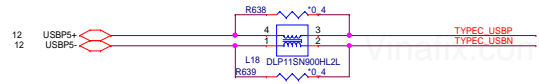
USB HOST facing RX channel
receiver equalization setting; Internal tied to VDD33/2, 3.3V I/O.
SSEQ =
L: Programmable EQ level#1
H: Programmable EQ level#2
M: Programmable EQ level#3 (default)

DP Receiver equalization setting;
Internal tied to VDD33/2, 3.3V I/O.
DPEQ =
L: Programmable EQ level#1
H: Programmable EQ level#2
M: Programmable EQ level#3 (default)

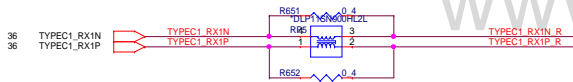
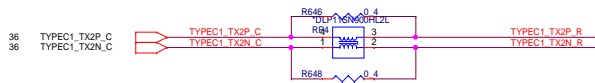
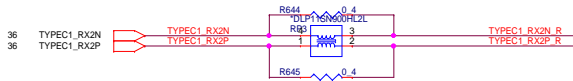
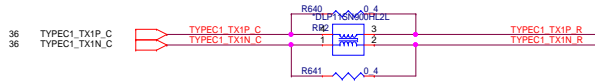
ADDR1, ADDR0: I2C control bus address LSB; Internal pull down at 150k-200k, 3.3V I/O.
[DPREQ, SSEQ] =
LL: 0x20/0x21 (default)
LH: 0x22/0x23
HL: 0x32/0x33
HH: 0x34/0x35

PS8740B I2C Control Mode

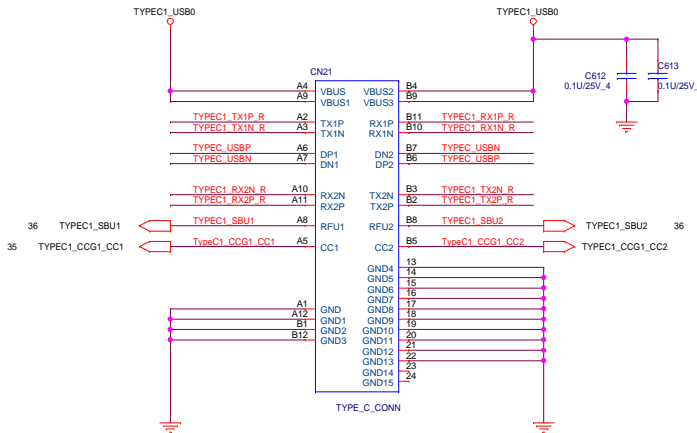
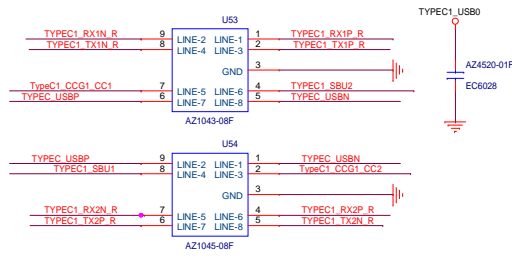
USB2.0 ESD



Type C1_HSIO_ESD

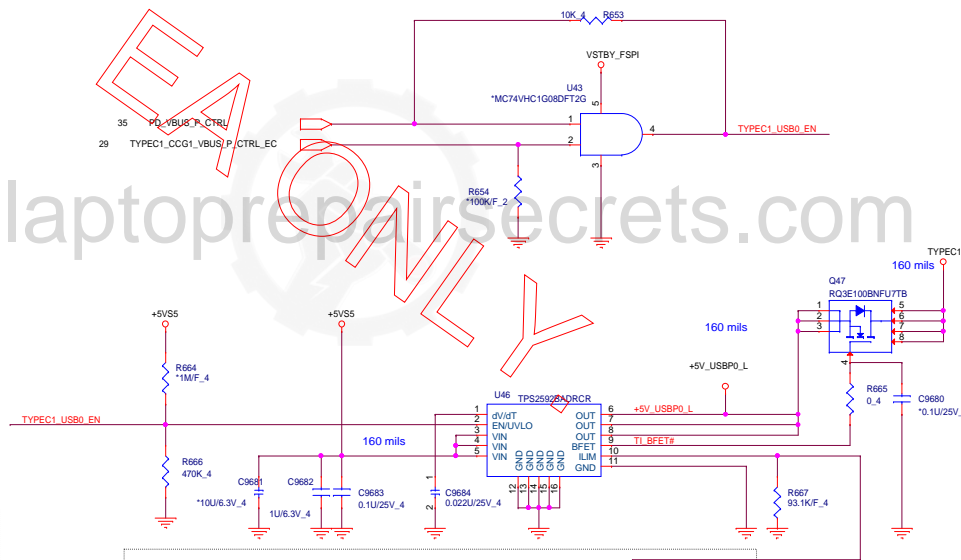


EC-SIT-27



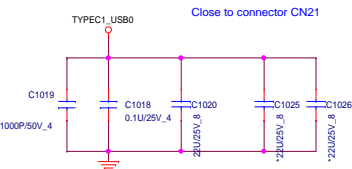
4,19,26,27,28,32,33,35,38,41,42,45,46,47,48,49,51
+5VSS
52 TYPEC1_USB0
29,38,52 VSTBY_FSP1

37



$$R_{lim} = (I_{lim} - 0.7) / (3 * 0.00001)$$

EC-FVT-08



USB INTERFACE

38

EC-DV-08

EC-SIT-02

EC-SIT-11

EC-FVT-05

Dead battery function

EC-SIT-26

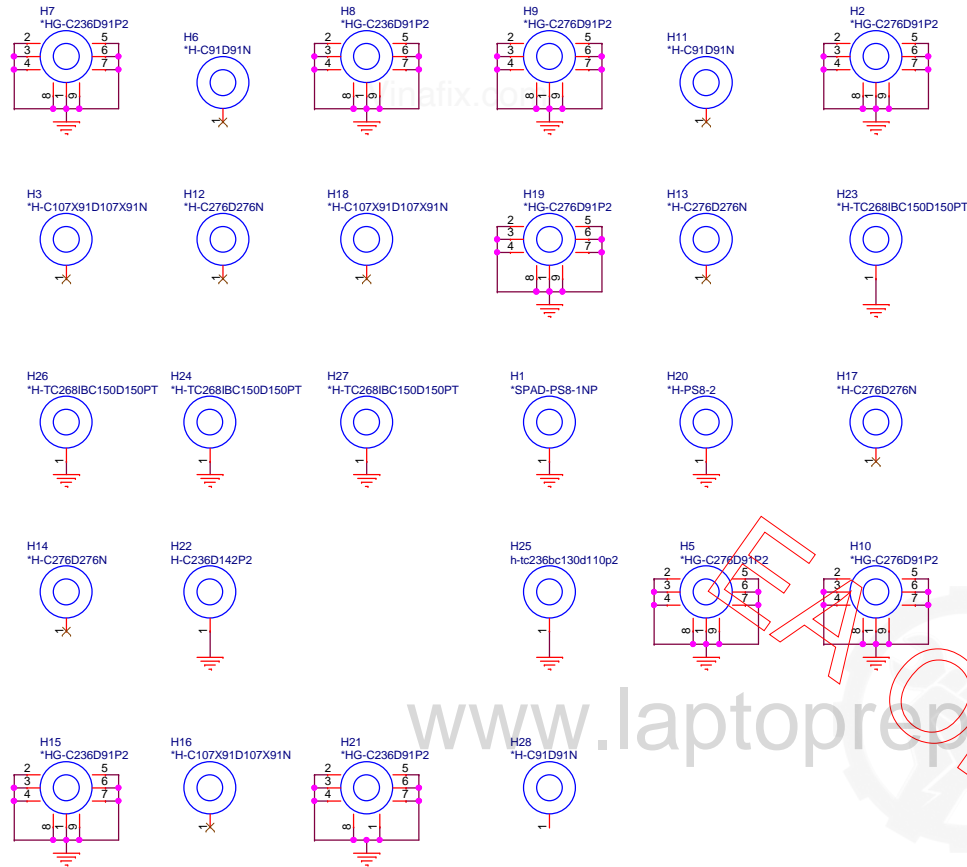
EC-SVT-01

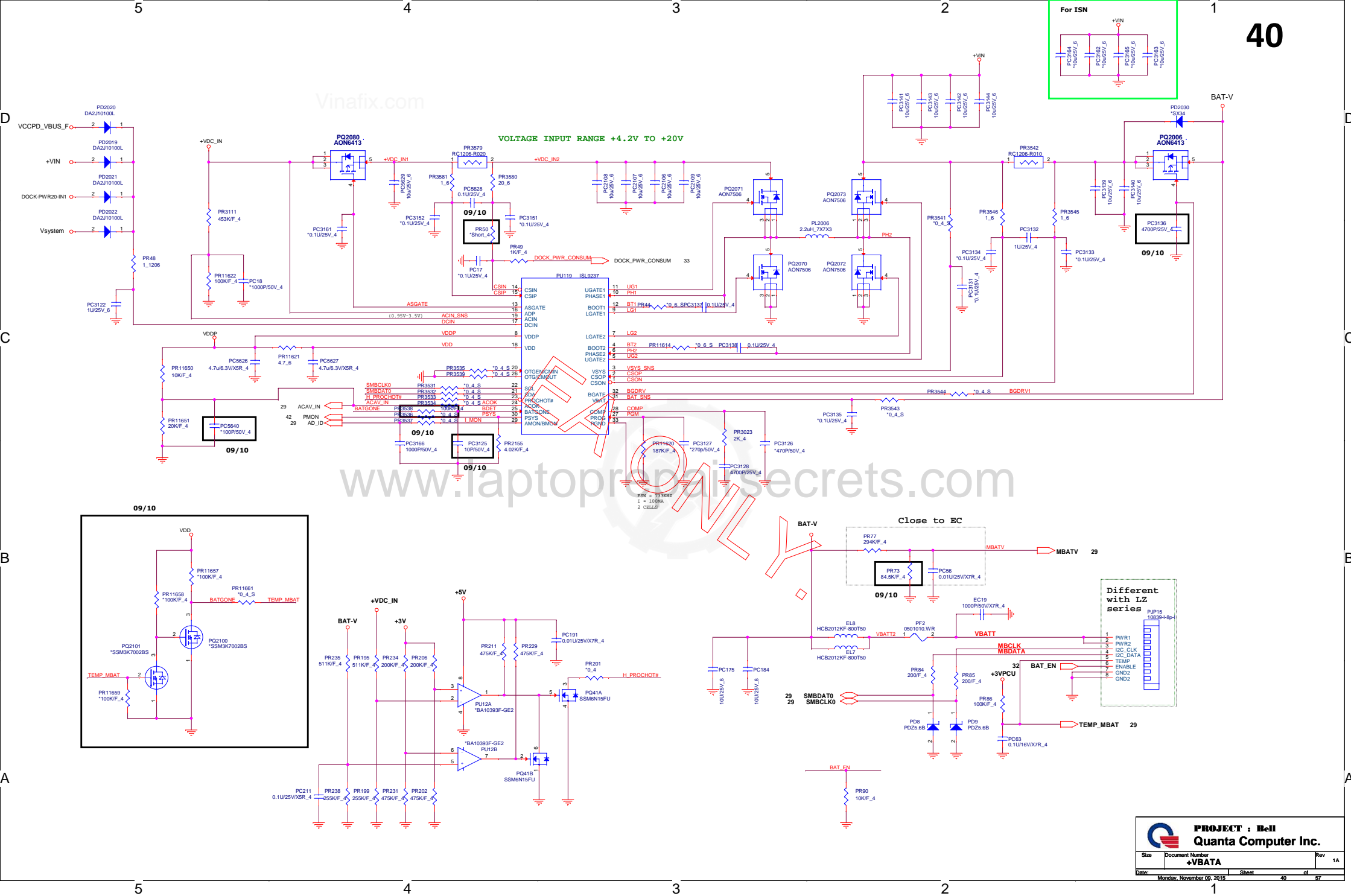
3.54V

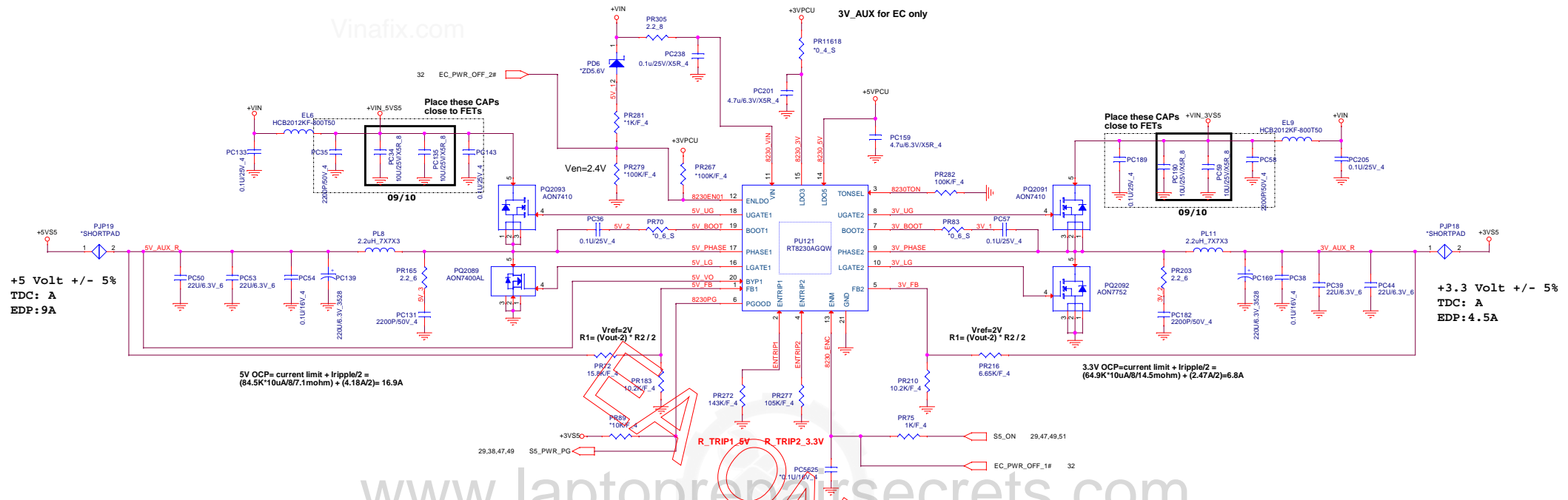
EC-FVT-07

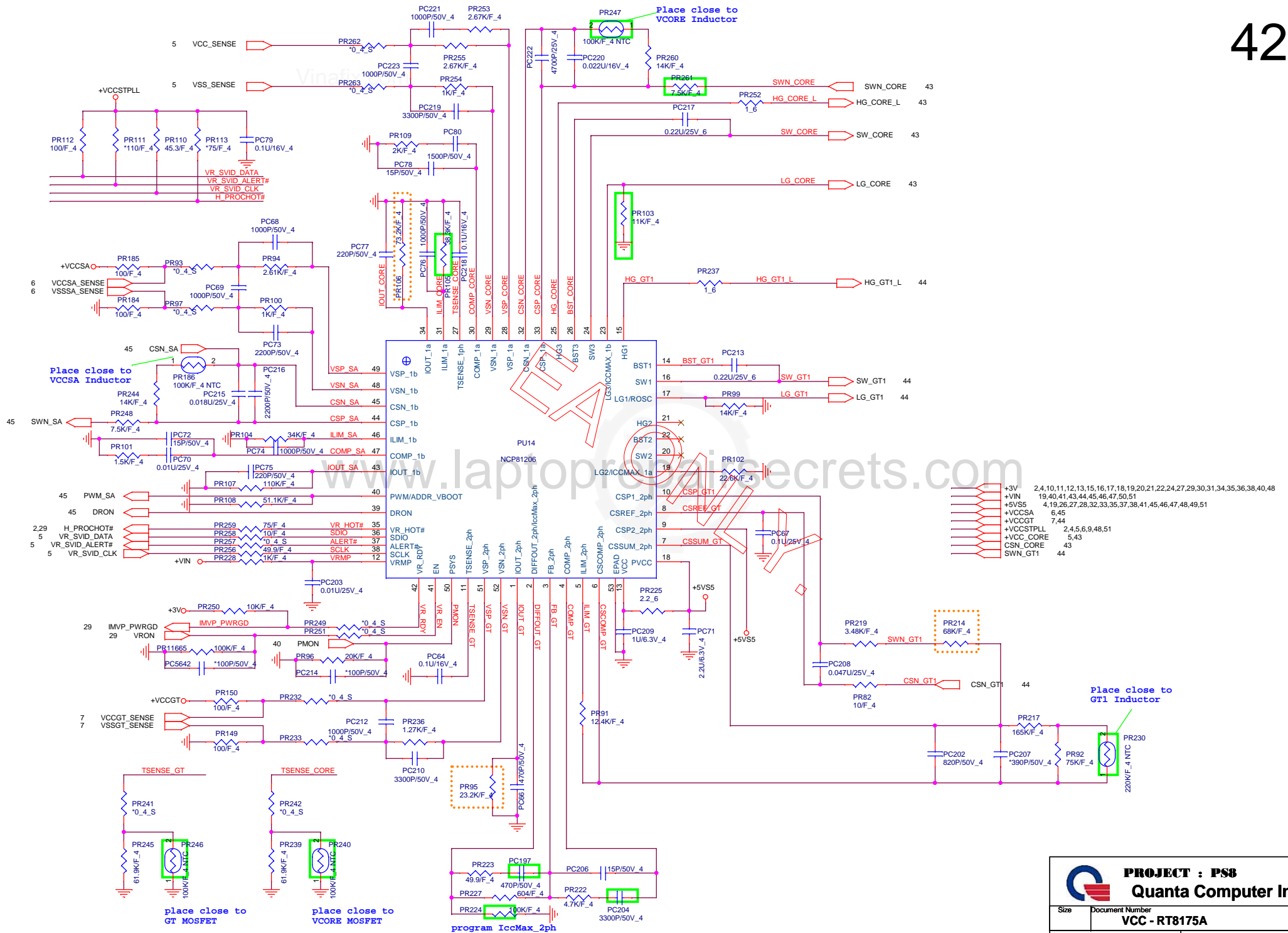
3.54V

EC-SVT-01

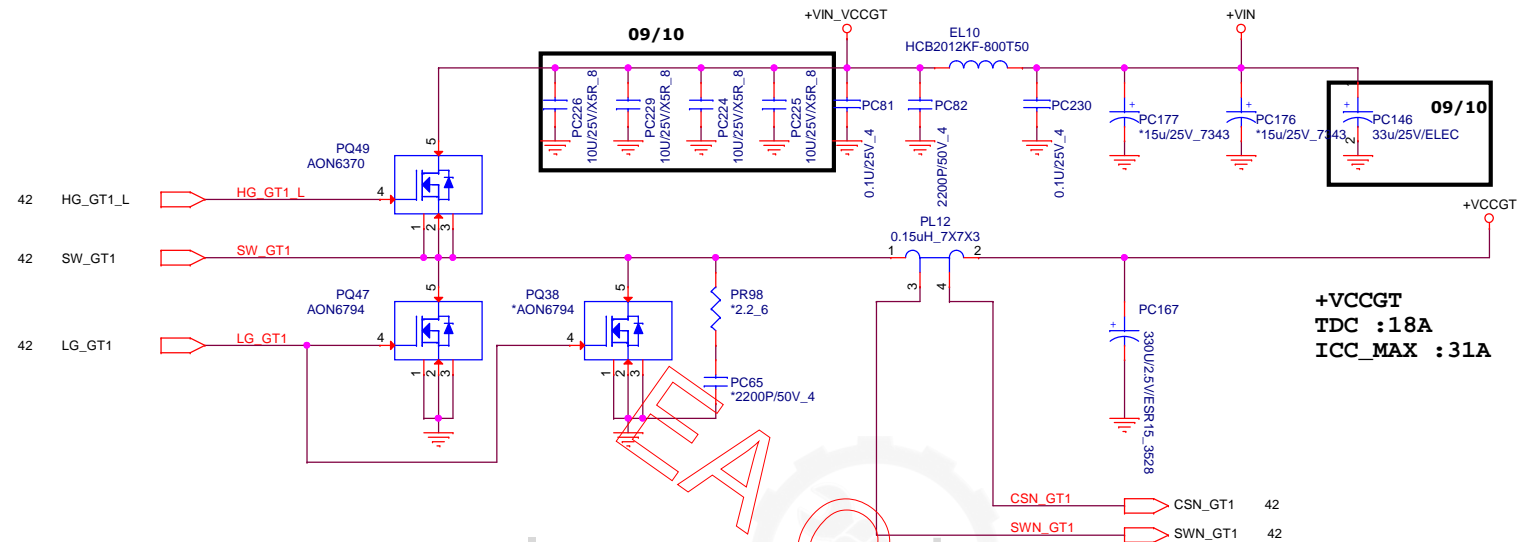











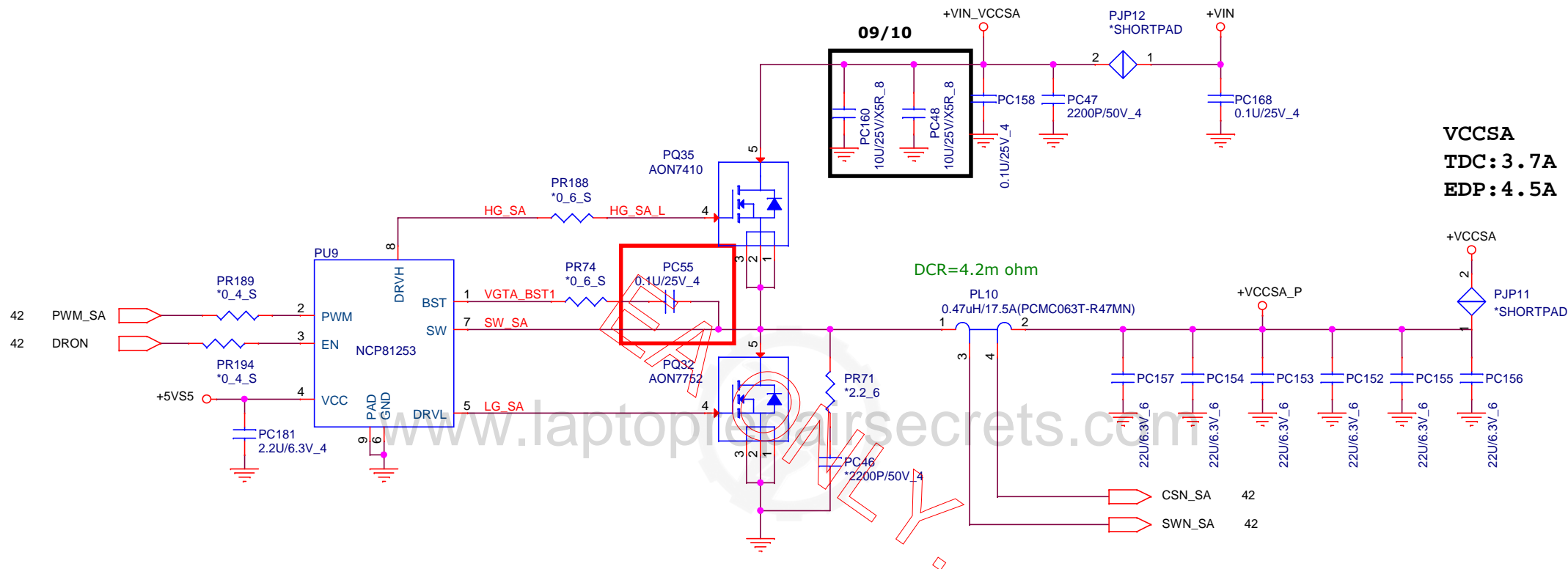


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VCCSA

Vinafix.com

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Quanta Computer Inc.

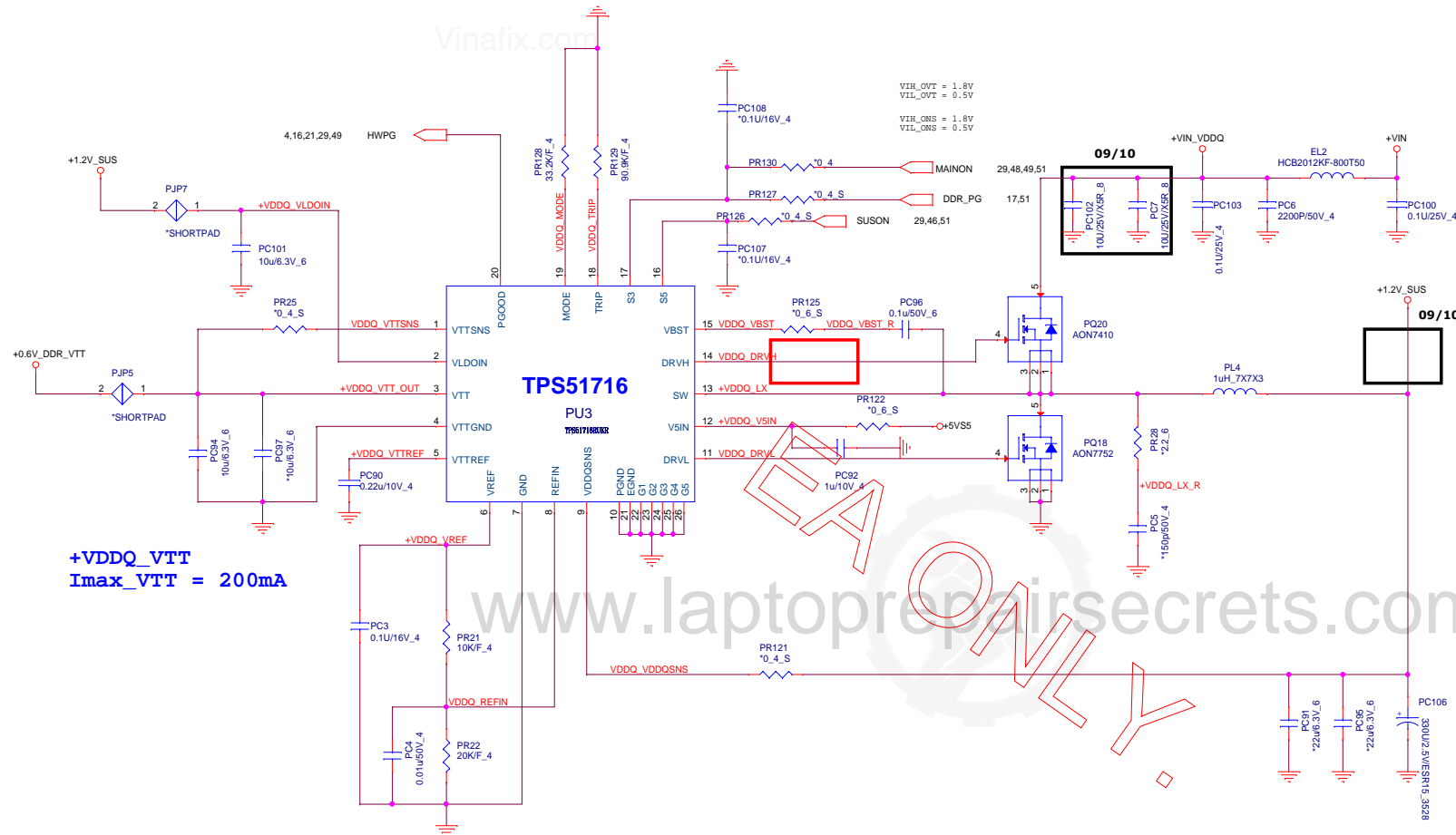
6	Document Number	Rev	<RevCode>
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$F_{sw}=500\text{kHz}$

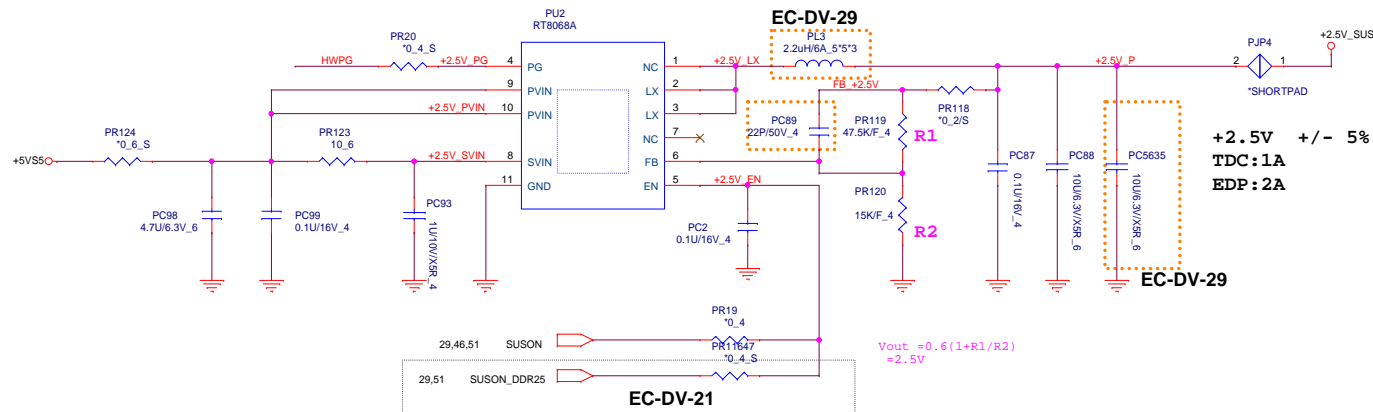
```

19,40,41,42,43,44,45,47,50,51      +VIN
4,19,26,27,28,32,33,35,37,38,41,42,45,47,48,49,51      +5VS5
2,4,10,11,12,13,15,16,17,18,19,20,21,22,24,27,29,30,31,34,35,36,38,40,42,48      +3V
3,6,17,18,51      +1.2V_SUS
17,18,51      +0.6V_DDR_VTT

```



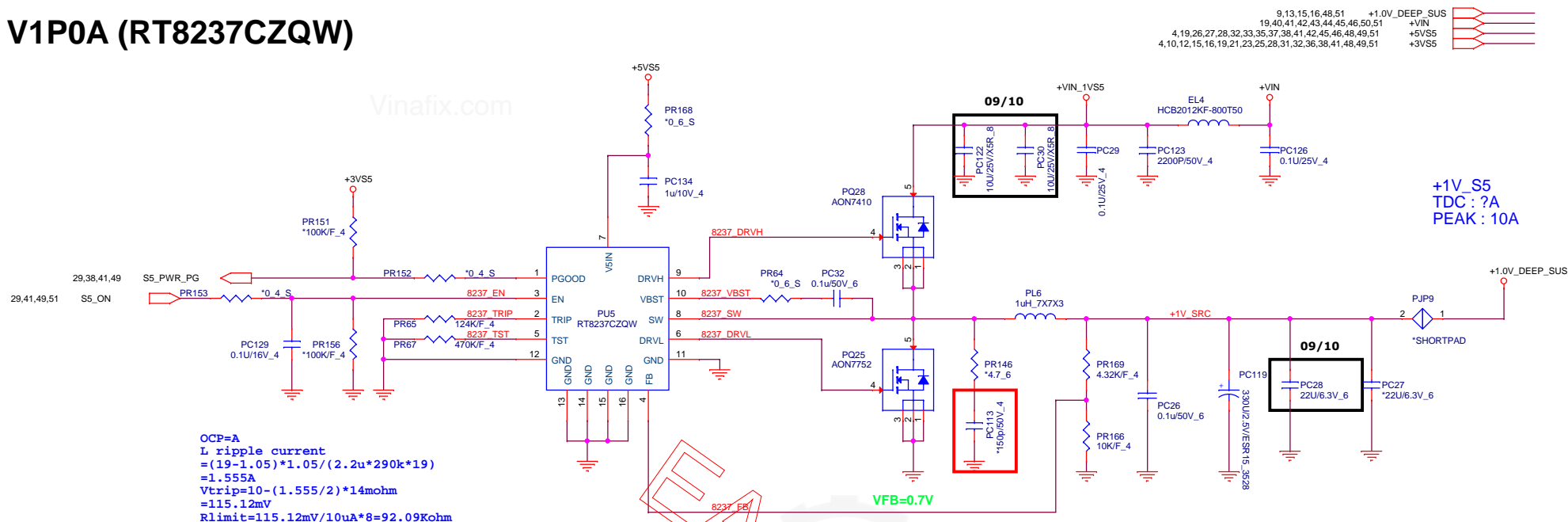
```
+1.2V_SUS
TDC: A
EDP:5.5A
```



+2.5V +/- 5%
TDC:1A
EDP:2A

$$V_{out} = 0.6(1 + R_1/R_2) = 2.5V$$

V1P0A (RT8237CZQW)

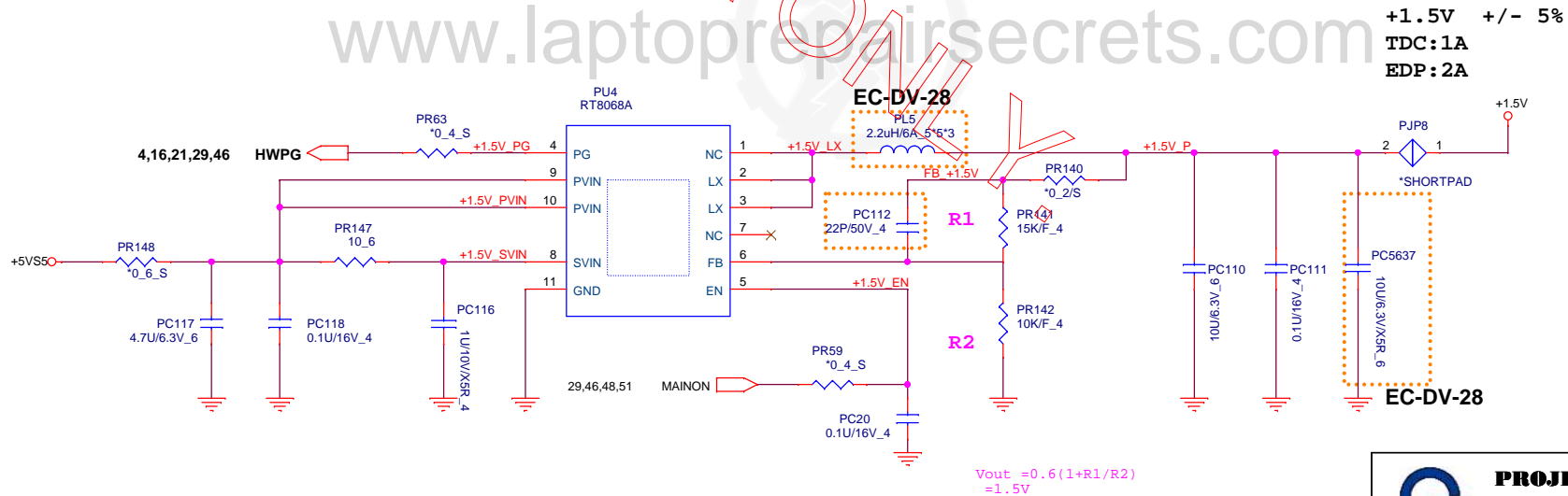
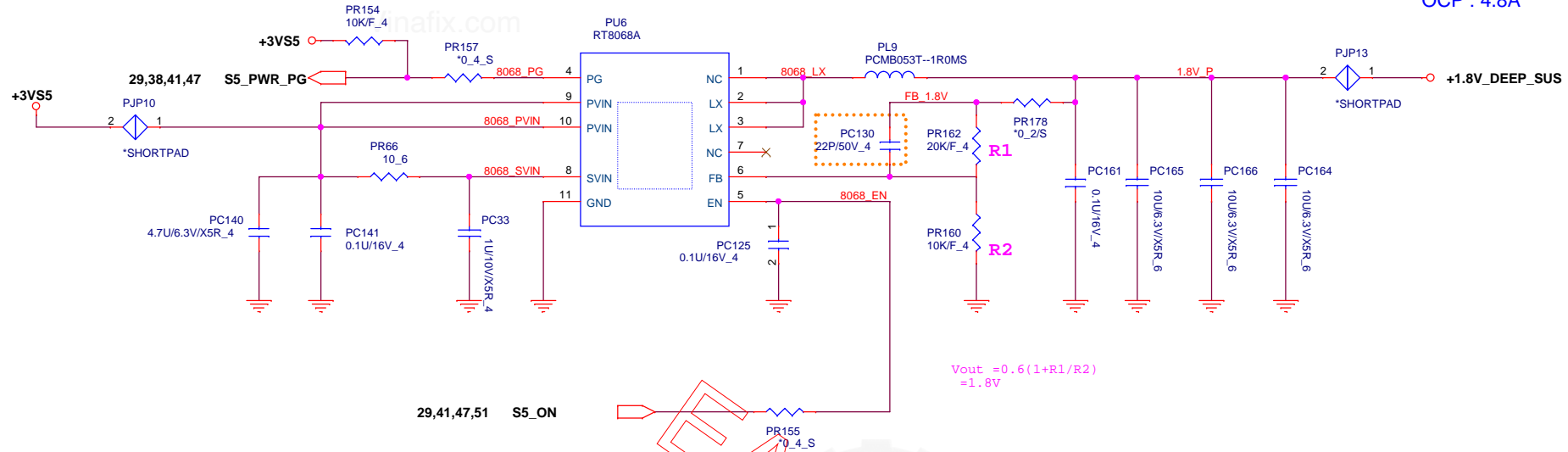



www.laptoprepairsecrets.com

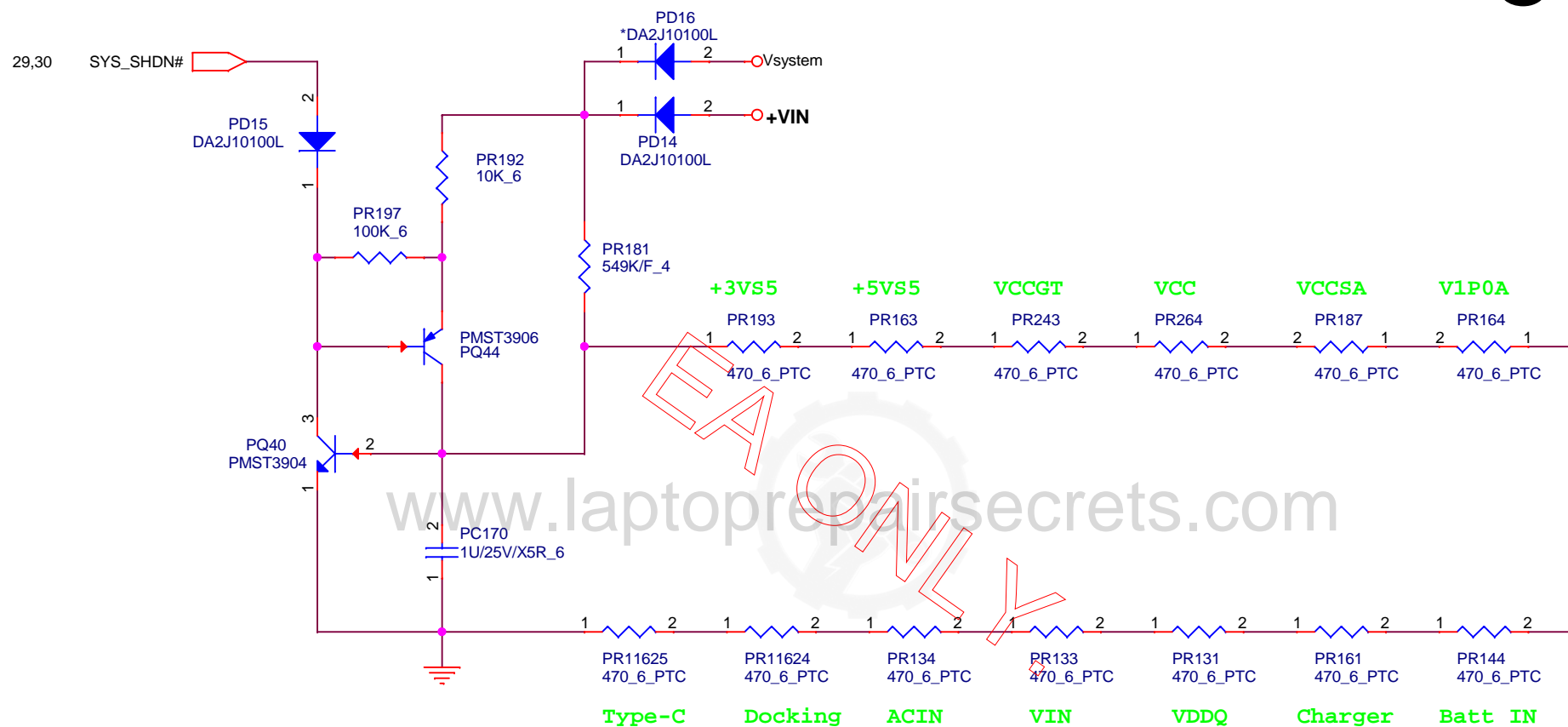
V1P8A (RT8068A)


1.8V_S5
Fsw : 900KHz
PEAK : 0.27A
OCP : 4.8A

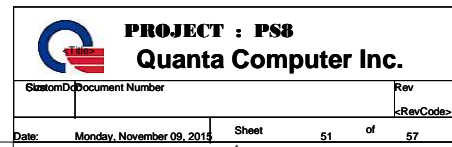
49

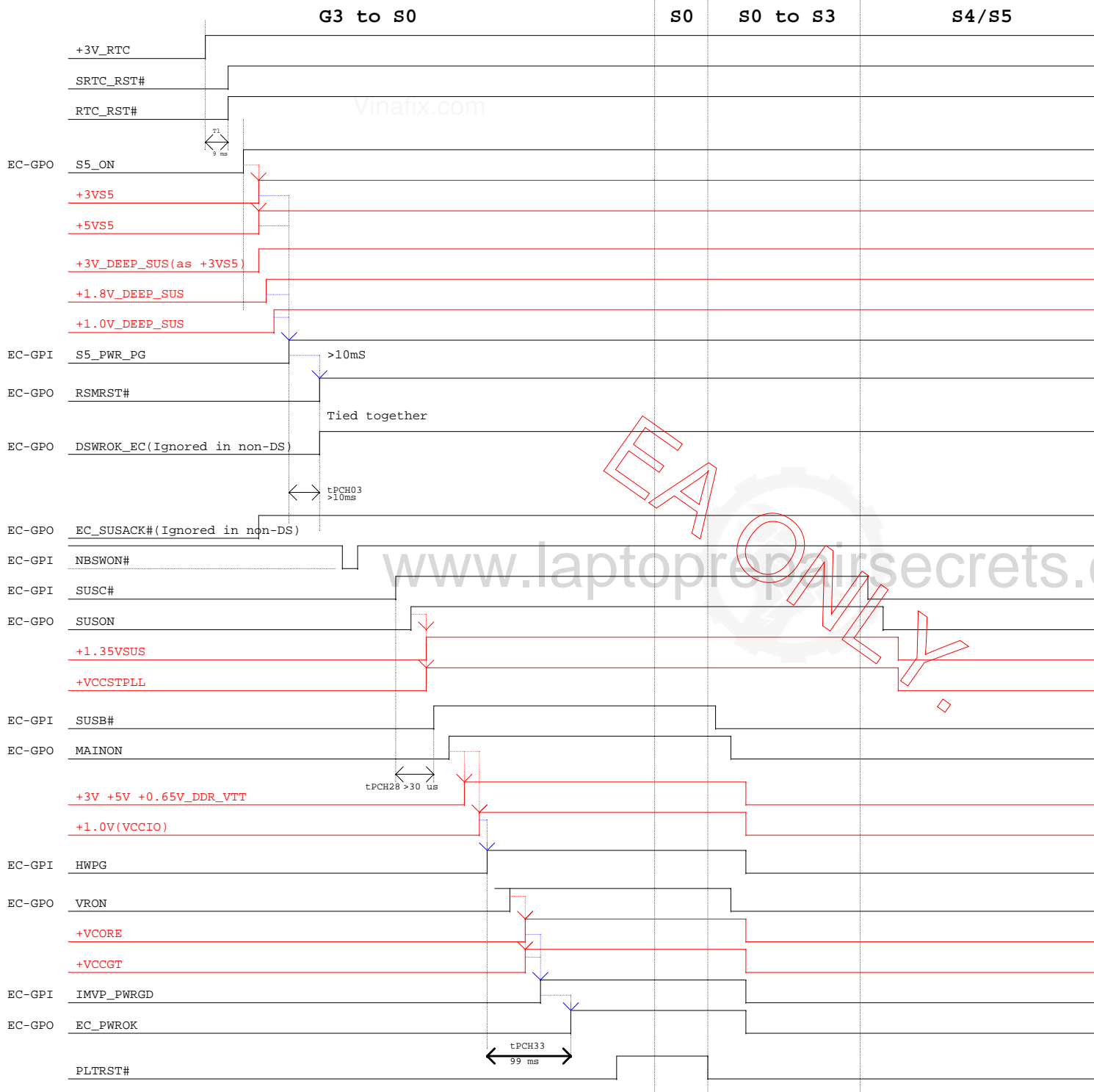


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DV-STAGE

2015	EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
	EC-DV-01	33	07/21	PQ2069,PQ6,EL5,EL12,PQ4	Move Dock power switch to page 52
	EC-DV-02	26	07/21	C530,C531,C532,C533,C534,C535,C536,C537,C538,C539,C540,C541,C542,C543,C544,C545,C546,C547,C548,C549,C550,C551,C552,C553,C554,C555,C556,C557,C558,L17,R543,R544,R545,R546,R547,R548,R549,R550,R551,R552,R553,R554,R555,R556,R557,R558,R559,R560,U37,Y4,R555,R561	USB3.0 two ports change to USB HUB solution
	EC-DV-03	12	07/21	U28	USB OC & PORT change
	EC-DV-04	34	07/21	U38 and Page 34 Related Parts	Change DP design from DP repeater to DP 1to 2 switch
	EC-DV-05	35~37	07/21	U49 and Page 35/36/37 Related Parts	Add USB Type-C solution
	EC-DV-06	2	07/31	R721	Add R721 resistor for DDI port C HW Strap
	EC-DV-07	4	07/31	R128	Remove the pull up resistor
	EC-DV-08	38	07/31	CN25,R751,R752	Add FPR_swipe solution
	EC-DV-09	12,19	07/31	F1,C108,Q15,C9714,R737,R47,Q3	Reserve USB Touch Panel Function
	EC-DV-10	19	07/31	CN23	Change LCD Connector to 40 Pin
	EC-DV-11	23	07/31	R239,R748,C278	Fine tune LAN power soft start circuit
	EC-DV-12	10	08/02	R723	Reserve a pull up resistor
	EC-DV-13	19	08/02	R394,R378,C9715	Fine tune Camera power soft start circuit
	EC-DV-14	30	08/02	D22,R231	Fine tune the thermistor citcuit
	EC-DV-15	31	08/02	R372,R373	Change TP SMBUS pull up to 3.3V
	EC-DV-16	40	08/14	Page 40	Charger IC solution change to ISL9237HRZ-T
	EC-DV-17	41	08/14	Page 41	3V/5V IC solution change to RT8230AGQW (Support 5V output 9A)
	EC-DV-18	52	08/14	Page 52	All power switch Move to page 52

	EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
2015 FVT-STAGE	EC-FVT-01	16	08/14	CN3	XDP CONNECTOR PIN DEFINE CHANGED
	EC-FVT-02	17,18	08/14	C1,C18	Change DDR3_DRAMRST# C to 0.1u
	EC-FVT-03	29,46	08/14	U34,PR19 and PR11647	CHANGE DDR3 2.5V POWER SEQUENCE TO MEET SPEC.
	EC-FVT-04	14	08/14	U28	MOVE CAP_LOCK_LED TO BIOS CONTROL
	EC-FVT-05	38	08/14		REMOVE 8 PIN FP CONNECTOR
	EC-FVT-06	29	08/17	R662,R663	REMOVE DOUBLE PU FOR CCG_I2C_SCL/DATA
	EC-FVT-07	35,38	08/17	U51 AND RELATE PARTS	Separate DEAD BATTERY/CCG2 AND EC POWER
	EC-FVT-08	29,37	08/17	R759,Q51,R757	ADD 1.5A CONTROL FOR TYPEC USB POWER OUTPUT SELECT
	EC-FVT-09	34	08/17	Q52,R761,R762	RESERVE I2C INTERFACE FOR DP SWITCH
	EC-FVT-10	45	08/17	PL5,PC5637	Improve +1.5V circuit
	EC-FVT-11	45	08/17	PL3,PC5635	Improve +2.5V_SUS circuit
SIT-STAGE	EC-SIT-01	26	09/14	U52 AND RELATE PARTS	Change to 4 port solution due to reserve to support TS panel
	EC-SIT-02	38	09/14	CN25	FINGER PRINT PIN DEFINE CHANGE
	EC-SIT-03	35	09/14	Q45	Q45 CHANGE TO P-MOS TO MEET CRB.
	EC-SIT-04	36	09/14	C610,C611	Change to 0 ohm
	EC-SIT-05	34	09/14	R568,R104,R123,R562,R563,R566	POP for auto detect type- c and onelink DP plug-in / FINE TUNE FOR VENDOR SUGGESTION
	EC-SIT-06	38	09/14	PC5631,C9721,R779	RESERVE SOFT START FOR CCG2 DEAD BATTERY CIRCUIT.
	EC-SIT-07	32	09/14	LED1	Change LED pin define.
	EC-SIT-08	9	09/14	R781	FOR VSS TIE TO GND
	EC-SIT-09	6	09/14	R784,R513	FOR POWER SEQUENCE(RESERVE)
	EC-SIT-10	19	09/24	U24,R814	FOR ECSL source
	EC-SIT-11	38	09/25	CN25,CML14,U28	USB PORT 8 P/N REVERSE
	EC-SIT-12	34	09/25	R573~R577,Q37~Q39	REMOVE FOR NON-HDMI SUPPORT
	EC-SIT-13	12	09/25	C470~C475	POP
	EC-SIT-14	4,19	09/25	R815	FOR TOUCH PANEL ENABLE PIN



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2015

SIT-STAGE

EC NO.	PG.	DATE	PART REFERENCE	DESCRIPTION
EC-SIT-15	40	09/30	1. PR11661 2. PC5640 3. PR73	1. Modify function for battery gone 2. Reserve bypass capacitor 3. Adjust battery detect voltage
EC-SIT-16	41	09/30	PC34 、PC135 、PC59 、PC190	Change capacitor for VIN transient
EC-SIT-17	43	09/30	PC227 、PC83 、PC228 、PC84	Change capacitor for VIN transient
EC-SIT-18	44	09/30	PC226 、PC229 、PC224 、PC225, PC146	Change capacitor for VIN transient
EC-SIT-19	45	09/30	PC160, PC48	Change capacitor for VIN transient
EC-SIT-20	46	09/30	1. PC102, PC7 2. Remove PJP6 *SHORTPAD	1. Improve VIN transient 2. EE request to increase "+1.2V_SUS" plane
EC-SIT-21	47	09/30	1. PC122, PC30 2. PC28	1. Improve VIN transient 2. Improve ripple
EC-SIT-22	52	09/30	1. PR283, PQ26, PQ2069, PR540, R537, R536, PR32, PQ22, PR4 , PR6, PR9 and PQ2082, add PC5638, PC5639 2. Add PD2032, PD2033, PQ2099, PR11653 , Pr11654, PR11655, PR11656, PR11663	1. Not shutdown when DCIN and DOCK switch 2. Avoid leakage voltage
EC-SIT-23	52	09/30	R733, PR11611	Modify DOCK ID detect
EC-SIT-24	32	09/30	C9751	Reserve for LG battery issue.
EC-SIT-25	15	09/30	L21,C9752	POP FOR RF SOLUTION
EC-SIT-26	38	10/01	PR11664	FOR DEAD BATTERY FUNCTION/ CC1,2 RISING SAME AS CCG2 3V
EC-SIT-27	37	10/02	U53,U54,EC6028	ESD CHANGED SLOUTION
EC-SIT-28	29,35	10/02	R662,R663,R731,Q57,Q58	TO SOLVE LEAKAGE PROBLEM
EC-SIT-29	26	10/06	R655~R659,C615,U45	POP TO LET EC CAN CONTROL USB HUB BY SMBUS INTERFACE/ RESERVE TO FINE TUNE STRENGTH
EC-SIT-30	14,38	10/06	R828,R829,Q59,Q69,C9753,C9754,R830	LET BIOS CAN TURN ON/OFF FP BY THEMSELVES
EC-SIT-31	13,23	10/06	C441,C445,C450,C454,C478,C479	FINE TUNE TO MEET VENDOR SUGGESTION
EC-SIT-32	6	10/08	R196,R199	Does not apply when rails are merged form PDDG info.



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Quanta Computer Inc.

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